(EFFECTIVE FROM ACADEMIC YEAR 2017-18)

Scheme of Teaching for III Semester B.E (E & C) (2016 Batch)

Subject Code	Title	Teaching Dept.	Contact hours/week				Examination		
			Theory	Tutorial	Practical	No of credits	CIE	SEE	Total Marks
MA31	Engineering Mathematics-III	Mat	03	02	00	04	50	50	100
EC31	Analog Electronics Circuits	EC	04	00	00	04	50	50	100
EC32	Digital Design	EC	04	00	00	04	50	50	100
EC33	Electrical Circuit Analysis	EC	03	02	00	04	50	50	100
EC34	Electronic Instrumentation and Measurements	EC	03	00	00	03	50	50	100
EC35	Signals & Systems	EC	03	02	00	04	50	50	100
ECL36	Analog Electronics Circuits Lab	EC	00	00	03	1.5	50	50	100
ECL37	Digital Design Lab	EC	00	00	03	1.5	50	50	100
		TOTAL	**20**	**06**	**06**	**26**	**450**	**450**	**900**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(EFFECTIVE FROM ACADEMIC YEAR 2017-18)

Scheme of Teaching for IV Semester B.E (E & C) (2016 Batch)

Subject Code	Title	Teaching Dept.	Contact hours/week				Examination		
			Theory	Tutorial	Practical	No of credits	CIE	SEE	Total Marks
MA41	Engineering Mathematics-IV	Mat	03	02	00	04	50	50	100
EC41	Microprocessor and Microcontroller	EC	03	02	00	04	50	50	100
EC42	Control Systems	EC	04	00	00	04	50	50	100
EC43	Fields and Waves	EC	03	02	00	04	50	50	100
EC44	Verilog HDL	EC	04	00	00	04	50	50	100
EC45	Linear Integrated Circuits	EC	04	00	00	04	50	50	100
ECL46	Microcontroller Lab	EC	00	00	03	1.5	50	50	100
ECL47	HDL Lab	EC	00	00	03	1.5	50	50	100
		TOTAL	**21**	**06**	**06**	**27**	**450**	**450**	**900**

CHAIRMAN
BOS

DEAN
(ACADEMIC)

PRINCIPAL

Subject Title : Analog Electronic Circuits

Sub.Code: EC31 No. of Credits:4=4:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 Explain and Demonstrate the Diode Circuits, BJT Amplifier and its analysis using Hybrid Equivalent Model .
2 Recall FET characteristics, Analysis of different biasing schemes and also demonstrate FET Circuits using its equivalent model.
3 Demonstrate and Construct Frequency response of BJT and FET amplifiers at various frequencies.
4 Demonstrate and Apply Feedback to amplifier circuits using BJT and Oscillator circuits using FET.
5 Define, Demonstrate and Analyze Power amplifier circuits in different modes of operation and analysis of Voltage Regulators.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Diode Applications :** Clipping and Clamping circuits. **AC Analysis of BJT Circuits:** Transistor Models and Parameters-hybrid model of CB, CE and CC, definition of h-parameters, Common Emitter amplifier circuit Analysis with and without bypassed Emitter Resistor, Common Collector amplifier circuit Analysis. *TEXT 1 and TEXT 2.*	11	L1,L2,L3.L4
2	**FET Biasing:** Introduction, DC load line and Bias Point, Gate Bias, Self Bias, Voltage divider Bias, comparison of basic JFET bias Circuits, JFET Bias Circuit Design, Construction and Characteristics of Enhancement type and Depletion type MOSFETs. **AC Analysis of FET Circuits:** FET models and Parameters, Common Source amplifier circuit Analysis with and without bypassed Source Resistor, Common Drain amplifier Analysis. *TEXT 2 and TEXT 1.*	11	L1,L2,L3.
3	**BJT and FET Frequency Response:** Introduction, Logarithms, Decibels, General Frequency Considerations, Low-Frequency Analysis, Low-Frequency Response—BJT Amplifier, Low-Frequency Response—FET Amplifier Miller Effect Capacitance, High-Frequency Response—BJT Amplifier, High-Frequency Response—FET Amplifier, Multistage Frequency Effects. **Compound Configurations:** Introduction, Cascade, Cascode Connection, Darlington Connection (Theoretical Concept only). *TEXT 1 and TEXT 2.*	11	L1,L2,L3.
4	**Non sinusoidal Oscillator Circuits:** Transistor as a switch, Transistor switching times, factors affecting various time delays. Types of Multivibrators, circuit operation of astable multivibrators, switching times and frequency of oscillations, monostable multivibrator and bistable multivibrator. Applications of multivibrators. UJT characteristics and application as relaxation oscillator.	10	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	TEXT 1.		
5	**Power Amplifiers:** Introduction—Definitions and Amplifier Types, Series-Fed Class A Amplifier, Transformer-Coupled Class A Amplifier, Class B Amplifier Operation, Class B Amplifier Circuits, Amplifier Distortion, Power Transistor Heat Sinking, Class C and Class D Amplifiers. *TEXT 1.*	09	L1,L2,L3.

Note 1: Unit 2 and Unit 3 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Knowledge of working principles, characteristics and basic applications of Diodes and Transistors (BJT, FET and UJT). Knowledge of frequency response and Power amplifiers.

CO2 Analyse the Performance of BJT and FET amplifiers in different Configurations, Power amplifiers and non sinusoidal oscillator Circuits and also analyse diode clipping and clamping circuits.

CO3 Interpret the performance characteristics of transistors amplifiers and Oscillators.

CO4 Apply the knowledge gained in the design of Clippers, Clampers, transistorized circuits, amplifiers and Oscillators.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1, PO11, PO12

CO2 PO2, PO11, PO12

CO3 PO2, PO3, PO11, PO12

CO4 PO3, PO11, PO12

Text Books.

1 Robert Boylestad, Louis Nashelsky, "Electronic Devices and Circuit Theory", 10th edition, Prentice Hall Publishers, 2009

2 David A Bell, "Electronic Devices and Circuits", 5th edition, Prentice Hall Publishers, 2009

Reference Text Books.

1 J.Millman & C.C.Halkias, "Integrated Electronics Integrated Electronics", 2nd Edition, John Weily, 2010.

Web Links.

1 http://www.electronicshub.org/diode-clippers-and-clampers/.

2 www.daenotes.com › Electronics › Devices & Circuits.

3 www.onmyphd.com/?p=small.signal.model.

4 www.byjus.com/physics/feedback-amplifier-transistor-oscillator/.

5 www.learnabout-electronics.org/Amplifiers/amplifiers50.php.

6 www.circuitstoday.com/voltage-regulators

Subject Title : Digital Design

Sub.Code: EC32 No. of Credits:04=4:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 Ability to learn minimization techniques for logical expressions using Boolean laws and theorems, K-Maps, QM method and MEV methods.
2 Ability to design and realize combinational logic circuits and study of various logic families and their electric characteristics,
3 Ability to study and analyze the working principles of latches and Flip-Flops with timing consideration
4 Ability to study and design the sequential logic circuits.
5 Ability to learn, analyze and design of Mealy and Moore models sequential logic circuits

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Principles of combinational logic:** Simplification of logic expressions using Boolean laws and theorems. Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh Maps 3, 4 and 5 variables for both minterms and maxterms with don't care terms, Quine-McCluskey minimization technique- minterms, maxterms, and don't care terms, Map entered variables (MEV). **TEXT 1**	10	L1, L2
2	**Design of combinational logic:** General approach, Decoders-BCD decoders, Encoders. Digital multiplexers - Using multiplexers/Demultiplexer as Boolean function generators. Adders and subtractors- Cascading full adders, Look ahead carry adder, MSI Adder 7483, BCD Adder, parity circuit and comparators, 7485 IC. **Logic families:** Introduction to different logic families; Electrical characteristics of logic gates-logic levels and noise margins, fan-out, propagation delay, transition time, power consumption and power-delay product **TEXT 1 and TEXT 2**	10	L1,L2,L3.
3	**Sequential Circuits:** Basic Bi-stable Element, Latches- SR Latch, Application of SR Latch, A Switch Debouncer, The $\bar{S}\bar{R}$ Latch, The gated SR Latch, The gated D Latch, Timing considerations, The Master-Slave Flip-Flops- SR, JK, Edge Triggered Flip-Flops, Characteristic equations. **TEXT 2**	10	L1, L2, L3,L4
4	**Applications of sequential logic circuits:** Registers, Counters - Binary Ripple Counters, up/down counter. Synchronous Binary counters, Counters based on Shift Registers, Design of a Synchronous counters, Design of a Synchronous Mod-N Counter	10	L1, L2, L3, L4

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	using clocked JK, D, T, and SR Flip-Flops, Self correcting counters. **TEXT 2**		
5	**Sequential Design:** Introduction to Mealy and Moore Models, State Machine Notation, Synchronous Sequential Circuit Analysis. Construction of state Diagrams, Counter Design, Design with state equations **TEXT 2**	12	L1, L2

Note 1: Unit 2 and Unit 4 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Understand the minimization techniques of logical expressions

CO2 Understand the design principle of Combinational Logic circuits and various logic families.

CO3 Understand the sequential logic circuits such as Latches, Gated Latches and Various Flip-Flops with Timing consideration.

CO4 Applicaiton of sequential logic circuits such as Registers and Counters.

CO5 Analysis and Design of Melay and Moore models in sequential logic circuits.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2, PO3

CO2 PO2, PO3

CO3 PO2, PO3

CO4 PO4, PO5, PO11, PO12

CO5 PO2, PO3, PO11, PO12

Text Books.

1 John M. Yarbrough, **"Digital Logic, Application & Design**", , Thomson , 2002

2 R P Jain, "**Modern Digital Electronics**", Tata McGraw-Hill Education. , 2003

3 Donald D. Givone, "**Digital Principles and Design**", PHIMcGraw-Hill, 2003

4 M. Morris Mano, **"Digital Logic and Computer Design",** PHI**, 2005**

Reference Text Books.

1 John F. Wakerly**, "Digital Design Principles and Practice",** 3rd edition, Pearson Education**, 2002**

2 Charles Roth, Jr., Larry Kinney**, "Fundamentals Logic Design",** Cengage Learning, 6th Edition, **2009.**

3 M. Morris Mano**, "Digital",** Pearson Education**, 2006.**

4 Raj Kamal**, "Digital systems-Principles and Design",** Pearson education 2nd edition**, 2007**

Subject Title : Electrical Circuit Analysis

Sub.Code: EC33 No. of Credits:04=03:01:0 (L - T – P) No. of Lecture Hours/Week : 05
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:65

Course Learning Objectives:

1 Able toy to Understand and Analyze the basic concepts emphasizing Series and Parallel combination of passive and active Components, Source transformation and Source shifting Techniques. Able toy to apply the concept of Mesh and Nodal analysis techniques to analyze the Electrical networks
2 Able toy to Define the statements of circuit Theorems, and understand, analyze the network theorems to simplify the complicated electrical circuits..
3 Able toy to Understand and analyze the dynamic behaviour(DC Response) of electrical networks using initial and final conditions.
4 Able toy to Apply the Laplace Transforms to Electrical Circuits and Understand & analyze the mathematical model of electrical circuits with periodic and non periodic signals as inputs.
5 Able toy to Define various two port network parameters, Resonance and its applications.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Basic Circuit Concepts:** Ideal and Practical sources, Source transformations and source shifting, Network reduction using Star – Delta transformation, Loop and Nodal analysis with linearly dependent and independent sources for both DC and AC networks, Concepts of super node and super mesh analysis, Numerical examples. *TEXT 1 and TEXT 2.*	14	L1,L2,L3.L4
2	**Network Theorems:** Thevinin's Theorem, Norton's Theorem, Superposition Theorem, Reciprocity Theorem, Millman's Theorem, Maximum Power transfer theorem. Numerical examples **Resonant Circuits**: Series Resonance, Frequency Response, Q-factor, Bandwidth, Resonant Frequency, Derivation of frequency at which maximum voltage across L and C, Derivation of Maximum Voltage across L and C and Selectivity, Parallel Resonance Circuits, Frequency Response. Numerical Examples. *TEXT 2 and TEXT 1.*	14	L1,L2,L3.
3	**Transient Behavior and Initial Conditions:** Behavior of circuit elements under switching condition and their representation, Evaluations of initial and final conditions in RL, RC and RLC circuits only for DC excitations. *TEXT 1 and TEXT 2.*	13	L1,L2,L3.
4	**Laplace Transforms:** Step, Ramp and Impulse response of RL, RC, RLC series and parallel circuits with and without initial conditions. Waveform synthesis. *TEXT 2 and TEXT 1.*	12	L1,L2,L3.
5	**Two port network parameters:** Definitions of Z,Y,T and h-parameters, modeling of two port network parameters, relationship between two port network parameters, Condition of symmetry and reciprocity, Interconnection of two port networks. Numerical	12	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	problems. *TEXT 2 and TEXT 1.*		

Note 1: Unit 2 and Unit 3 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Ability to understand the Concept of Mesh, Nodal analysis, two port network parameters and initial and final conditions of electrical circuit elements.

CO2 Ability to Analyze and evaluate the electrical Networks using Mesh, Node analysis techniques.

CO3 Ability to Apply the source transformation, sifting, Laplace transforms and basic theorems to reduce the electrical circuits and its analysis.

CO4 Ability to understand, analyze and Evaluate the dynamic behavior of Electrical networks using initial and final conditions.

CO5 Ability to Simplify and evaluate the two port network parameters and derivation of the relation between each parameters.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1, PO11, PO12

CO2 PO1, PO2, PO11, PO12

CO3 PO1, PO2, PO3, PO11, PO12

CO4 PO1, PO2, PO3, PO11, PO12

CO5 PO1, PO2, PO3, PO11, PO12

Text Books.

1 M.E. Van Valkenberg, "Network analysis", 10th edition, Prentice Hall of india Publishers, 2000

2 Roy Choudhury, "Networks and systems", 2nd edition, New Age International Publications, 2006

3 Charles K Alexander and Mathew N O Sadiku, "Fundamentals of Electric Circuits", 3rd edition, Tata McGraw-Hill, 2009

Reference Text Books.

1 Hayt, Kemmerly and Durbin, "Engineering Circuit Analysis", 7th Edition, TMH, 2010.

2 J. David Irwin /R. Mark Nelms, "Basic Engineering Circuit Analysis", 8th Edition, John Wiley, 2006.

3 Charles K Alexander and Mathew N O Sadiku, "Fundamentals of Electric Circuits", 3rd Edition, McGraw-Hil, 2009.

4 A. Sudhakar and Shyam Mohan S Pillai, "E circuits and Networks ", 5th Edition, MC Graw Hill Education, 2015.

5 Ravish R Singh, "Electrical Networks", 2nd Edition, MC Graw Hill Education, 2009.

Web Links.

1 nptel.ac.in/courses/108102042/

2 gradestack.com/Circuit-Theory-and/Laplace...and.../19349-3926-40444-study-wtw

3 https://www.khanacademy.org/science/electrical-engineering/ee-circuit-analysis-topic

Subject Title : Electronic Instrumentation And Measurements

Sub.Code: EC34 No. of Credits:03=03:0:0 (L - T – P) No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:39

Course Learning Objectives:

1 To study and analyze the different types of errors, measurement of Voltage & Power
2 To study the different digital instruments.
3 To study the different types of signal generators and to understand the concept of CRO measurement.
4 To study the measurement of R, L and C using bridge networks.
5 To understand the concept of different transducer.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	Errors in Measurement: Gross errors and systematic errors, Absolute and relative errors, Accuracy, Precision, Resolution and Significant figures. Ammeters: DC Ammeter, Multirange Ammeter, The Ayrton Shunt or Universal Shunt, Requirements of Shunt, Extending of Ammeter Ranges, RF Ammeter(Thermocouple). Voltmeters: Introduction, Multi range voltmeter, Extending voltmeter ranges, Loading, AC voltmeters using Rectifiers – Half wave and full wave, Peak responding and True RMS voltmeters. TEXT 1 and TEXT 2	09	L1,L2,L3.
2	Digital Voltmeters: Introduction, Ramp technique, Dual slope integrating type DVM(V – T conversion) , Integrating type DVM(V – F conversion), Successive approximations, 3 ½ digit, Resolution and Sensitivity of Digital Meters. Digital Instruments: Introduction , Digital Multimeters, Digital frequency meters, Digital measurement of time. TEXT 1	07	L1,L2,L3.
3	Signal Generators: Introduction, Fixed and variable AF oscillator, Standard signal generator, Modern Laboratory signal generator, AF sine and Square wave generator, Function generator, Square and Pulse generator, Sweep frequency generator, Frequency synthesizer. Oscilloscope: Introduction, Basic principles, CRT features, Block diagram of Oscilloscope, Simple CRO, Vertical Amplifier, Horizontal Deflecting System-Sweep or Time Base Generator. TEXT 1 and TEXT 2	08	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
4	Bridges: Introduction,Whetstone's bridge, Kelvin Bridge, AC bridges, Capacitance Comparison Bridge, Maxwell's bridge, Wien's bridge, Wagner's earth connection. TEXT 1	07	L1,L2,L3.
5	Transducers: Introduction, Electrical transducers, Selecting a transducer, Resistive transducer, Resistive position transducer, Resistance thermometer, Thermistor, Differential output transducers and LVDT, Piezo electrical transducer, photoelectric transducer, Semiconductor photo diode . Display devices: Digital display system and Indicators, classification of displays, Display devices, LEDs, LCD displays.TEXT 1	08	L1,L2,L3.

Note 1: Unit 1 and Unit 5 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Define and Identify different types of errors.

CO2 Estimation of Voltage, Power, R, L and C.

CO3 Determine the parameters for power bridges.

CO4 Analyze and compare the types of Signal generators, Displays and transducers.

CO5 Design voltmeter and bridge circuits,and Analyze Spectrum Analyzers.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2

CO2 PO1,PO2

CO3 PO1,PO2,PO6

CO4 PO1,PO2

CO5 PO1,PO2,PO6

Text Books.

1 H. S. Kalsi,, "Electronic Instrumentation,", Sixteenth reprint, TMH Publisher, 2009

2 David A Bell, "lectronic Instrumentation and Measurements"", PHI / Pearson Education, 2006.ion

Reference Text Books.

1 Cooper D & A D Helfrick, , ""Modern electronic instrumentation and measuring techniques", PHI, 2003. ", edition, PHIr, 2003

2 A K Sawhney ""Electronics & electrical measurements",", 18th edition, , Education and technical publishers, 2008

Web Links.

1 http://nptel.ac.in/ online course /electronic_ instrumentation _measurements

2 https://books.google.co.in/books/about/electronic_instrumentation _measurements

3 https://www.youtube.com/watch?v=oOMlwW4rBz8/DavidBell

4 Author Name, " Text Book title", Edition of the Text Book, Publisher Name, Year of the Publication

5 Author Name, " Text Book title", Edition of the Text Book, Publisher Name, Year of the Publication

Subject Title : Signals And Systems

Sub.Code: EC35 No. of Credits: 4=3 : 1 : 0 (L-T-P) No. of Lecture Hours/Week : 5
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:65

Course Learning Objectives:

1 Define and identify the Continuous-time and Discrete time signals and systems.
2 Summarise and distinguish the time domain representations for LTI systems.
3 Apply the concepts of frequency domain representation of signals and its advantages.
4 Analyze and illustrate the properties of Fourier representations.
5 Define Z-transforms and illustrate the conversion from time domain to Z-domain.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Introduction:** Definitions of a signal and a system, Classification of signals, Basic operations on signals, Elementary signal: Exponential Signals, Sinusoidal Signals, Step function, Impulse function, and Ramp function. Systems viewed as Interconnections of operations, Properties of systems. **TEXT BOOK:1**	13	L1,L2,L3.
2	**Time-domain representations for LTI systems**: Introduction, Impulse response representations of LTI system, Properties of Impulse response representation for LTI system, Difference and Differential equation representation of LTI Systems, Block Diagram representations. **TEXT BOOK:1**	15	L2,L3,L4,L5
3	**Fourier representation for signals:** Introduction, Fourier representations for four classes of signals, Review of Discrete time periodic signals: The discrete time Fourier series; Review of Continuous time periodic signals: The Fourier series; Review of Discrete time non-periodic signals: The discrete time Fourier transform; Review of Continuous time non-periodic signals: The Fourier transforms. (Derivations excluded). **TEXT BOOK:1**	10	L1,L2,L3,L4
4	**Properties of Fourier representations:** Linearity and Symmetry properties, Time and Frequency shift properties, Differentiation and Integration properties**,** Convolution property, Multiplication property, Scaling properties, Parseval's relationships. **Applications of Fourier Representations:** Introduction, Frequency response of LTI systems, Fourier transform representation of periodic signals, Fourier transform representation of discrete time signals, Sampling.	14	L2,,L3,L4,L5

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	TEXT BOOK:1		
5	**Z-Transforms:** Introduction to Z – transform, Properties of ROC, Properties of Z – transforms, Inverse Z – transforms [Partial Fraction and Power Series Expansion methods]. Transform analysis of LTI Systems, Unilateral Z-Transform and its application to solve difference equations. **TEXT BOOK:1**	13	L1,L2,L3,L4,L5

Note 1: Unit 2 and Unit 5 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Define signals and list their classification, representations for classes of signals.

CO2 Explain the behaviour of signals and properties of LTI systems.

CO3 Determine the concepts of Fourier Series, Fourier Transform.

CO4 Analyse and illustrate the properties and application of Fourier series and Fourier Transform.

CO5 Review of Z-transform concept, properties and demonstrate the application of Z-transform.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1, PO2,PO5

CO2 PO1, PO2, PO6,PO7

CO3 PO1, PO2, PO4, PO6, PO7, PO12

CO4 PO1, PO2, PO6, PO7, PO12

CO5 PO1, PO2, PO6, PO7, PO12

Text Books.

1 Simon Haykin and Barry Van Veen, "Signals and Systems", Edition, John Wiley & Sons, 2001, Re-Print 2010.

Reference Text Books.

1 Alan V Oppenheim, Alan S, Willsky and A Hamid Nawab, "Signals and Systems", 2nd edition , Pearson Education Asia / PHI, 1997. Indian Reprint, 2002

2 M. J. Roberts, "Signals and Systems", McGraw-Hill, Reprint, 2005

3 V. Krishnaveni and A. Rajeswari, "Signals and Systems", Wiley India, Reprint , 2012

Web Links.

1 http://nptel.ac.in/downloads/117101055/

2 https://engineering.purdue.edu/ChanGroup/ECE302Notes/UCSD_ECE101.pdf

3 https://ocw.mit.edu/resources/res-6-007-signals-and-systems-spring-2011/lecture-notes/

Subject Title : Analog Electronic Circuits Laboratory

Sub.Code: ECL36 No. of Credits:1.5=0:0:1.5 (L - T – P) No. of Lecture Hours/Week :03
Exam Duration:03 Hrs CIE+Assignment +SEE=50+50=100 Total No.of Contact Hours:39

Course Learning Objectives:

1 Design, Assembling and Testing of Diode Rectifiers, Clippers and clamper Circuits and Zener Diode Voltage Regulator.
2 Design, Assembling and Testing of BJT/FET Amplifier, Emitter follower and oscillator circuits.
3 Design, Assembling, Testing and Evaluation of JFET/MOSFET Characteristics.

Sl. No.	***Experiment***	***No. of Hours***	***Blooms Taxonomy Level***
1	Design and set up the following rectifiers without filter and to determine ripple factor and rectifier efficiency: (a) Full Wave Rectifier and (b) Bridge Rectifier.	3	L1, L2, L3, L4
2	Design and set up the following rectifiers with C-filter and to determine ripple factor and rectifier efficiency: (a) Full Wave Rectifier and (b) Bridge Rectifier.	3	L1, L2, L3, L4
3	Conduct experiment to test single and double ended diode clipping Circuits	3	L2, L3, L4
4	Conduct experiment to test diode clamping circuits (positive and negative).		L2, L3, L4
5	Conduct an experiment on Zener Voltage Regulator and determine its line and load regulation.	3	L2, L3, L4
6	Conduct experiment to Compute the characteristic parameters of MOSFET	3	L2, L3, L4
7	Design and setup BJT RC Coupled CE Amplifier and obtain its frequency response, input impedance and output impedance.	3	L2, L3, L4
8	Design and set up the JFET CS amplifier and obtain its frequency response, input impedance and output impedance.	3	L2, L3, L4
9	Realize BJT Darlington Emitter follower and determine the gain, input and output impedances.	3	L2, L3, L4
10	Design and set-up the RC-Phase shift Oscillator using BJT and calculate the frequency of output waveform.	3	L2, L3, L4
11	Design and set-up the crystal oscillator circuit using BJT and determine the frequency of oscillation.	3	L2, L3, L4
12	Design and setup an astable multivibrator using BJT obtain its frequency of oscillation.	3	L1, L2, L3, L4
13	Design and setup UJT Relaxation oscillator obtain its frequency of oscillation.	3	L1, L2, L3, L4

Note : The experiments are to be carried using discrete components only.

CO1 Designing of Diode Circuits, BJT Circuits and FET Circuits.

CO2 Test Diode Circuits, BJT Circuits, FET Circuits and UJT Circuits.

CO3 Compute the characteristic parameters of n-channel MOSFET

Course Outcomes Mapping with Programme Outcomes.

CO1 PO4, PO11

CO2 PO4, PO11

CO3 PO4, PO11, PO12

Subject Title : Digital Design Lab

Sub.Code: ECL37 No. of Credits:1.5=0:1.5:0 (L - T – P) No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs CIE +SEE=50+50=100 Total No.of Contact Hours:39

Course Learning Objectives:

1 Enable the students to get practical experience in simplifying the logical expression and its realization using logic gates and its testing.
2 Ability to understand, design, Testing and Combinational logic circuits.
3 Ability to Understand to realize Combinational logic circuits using MSI IC's
4 Ability to Understand the Truth Table and Verifications of Flip-Flops
5 Ability to Design and Testing of Sequential Logic circuits such as Registers and Counters.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	Simplification, realization of Boolean expressions using logic gates.	3	L1, L2
2	Designing and testing of Binary to Gray code conversion and vice versa	3	L1,L2,L3.
3	MUX/DEMUX – use of 74153, 74139 for code converter and arithmetic circuits.	3	L1, L2, L3,L4
4	Use of Decoder chip(7447) to drive 7-Segment LED display and Priority encoder.	3	L1, L2, L3, L4
5	Designing and testing of Half/Full adder and Half/Full Subtractors using logic gates.	3	L1, L2
6	Realization of combinational logic circuits using 7483 and logic gates i. BCD to Excess-3 code conversion and vice versa. ii. Parallel adder/Subtractor.	3	L1,L2
7.	Designing and testing of One/Two bit comparator and study of 7485	3	L1,L2
8.	Truth table verification of Flip-Flops: SR, D, JK, MSJK and MST - type (Using logic gates)	3	L1,L2
9	Testing of 4 bit sequential circuit/ MOD – N counter(7490, 7493, 74190, 74192, 74193)	3	L1,L2
10	Designing and testing of 3 bit sequential circuit and MOD – N counter design (7476)	3	L1,L2
11	Shift Registers: SISO (Shift right), SIPO, PISO, PIPO, Shift left operations using 7495.	3	L1,L2
12	Designing and testing Ring counter/Johnson counter using 7495	3	L1,L2

Course Outcomes:

CO1 Demonstrates the truth table of various expressions and combinational circuits using logic gates.
CO2 Design, test and evaluate various combinational circuits such as adders, Subtracts, Multiplexers, De-Multiplexers.

CO3 Construction of Flip-Flops and its truth table verification

CO4 Construction of Various applications of Sequential logic circuits.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2, PO4, PO5, PO11, PO12

CO2 PO2, PO4, PO5, PO11, PO12

CO3 PO4, PO5, PO11, PO12

CO4 PO4, PO5, PO11, PO12

Text Books.

1 John M. Yarbrough, "**Digital Logic, Application & Design**", First Edition, Thomson , **2002**

2 Donald D. Givone, "**Digital Principles and Design**", 2nd edition, Tata Mcgraw Hill Education Pvt. , 2003

Choose an item.

Subject Title : MICROPROCESSOR AND MICROCONTROLLERS

Sub.Code: EC41 No. of Credits:04=03:01:0 (L - T – P) No. of Lecture Hours/Week : 05
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:5

Course Learning Objectives:

1 To learn the architecture of 8086, 8051 and MSP430 microcontroller..
2 To learn the Instruction set and Embedded C for MCS51.
3 Ability to write a ALP and C program for a given algorithm and implement the same.
4 To learn the I/O ports and interfacing techniques with MCS51
5 Ability to develop single chip solution using MCS51.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Introduction to microprocessors and microcontrollers:** RISC & CISC CPU Architectures, Harvard & Von- Neumann CPU architecture. **The 8086 Processors:** 8086 Architecture, CPU Architecture-BIU and EU, Register organization, Memory organization and segmentation, pin functions of 8086. **TEXT 1 and TEXT 2**	08	L1,L2,L3.L4
2	**8051 Microcontroller:** The 8051 Architecture, Pin diagram of 8051, Memory organization, External Memory interfacing. Classification of Instruction, Addressing modes: Immediate addressing, Register addressing, Direct addressing, Indirect addressing, relative addressing, Absolute addressing, Long addressing, Indexed addressing, Bit inherent addressing, bit direct addressing. **TEXT 2**	12	L1,L2,L3.
3	**8051 Instructions and Programming:** 8051 instructions, Data transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instruction. 8051 programming: Assembler directives, Assembly language programs and Time delay calculations. Stack operations. Introduction to Embedded C, C data types, logical operations, programming 8051 using embedded C. **TEXT 2 and TEXT 3**	15	L1,L2,L3.
4	**Timers/counters:** 8051 timers/counters, programming 8051 timers in assembly and C. Data communication, Basics of Serial Data Communication, 8051 Serial Communication, connections to RS-232, Serial communication Programming in assembly and C. 8051 Interrupts and Basics of interrupts, 8051 interrupt structure, 8051 Interfacing and Applications: Basics of I/O concepts, I/O Port Operation, Interfacing 8051 to LCD, Keyboard, parallel and serial ADC, DAC, Stepper motor interfacing and DC motor interfacing and programming. **TEXT 3**	20	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
5	**MSP430microcontrollers:** Low Power embedded systems, On-chip peripherals (analog and digital), low-power RF capabilities. Target applications (Single-chip, low cost, low power, high performance system design). **MSP430 RISC CPU architecture,** Compiler-friendly features, Clock system, Memory subsystem. Key differentiating factors between different MSP430 families. **TEXT 4**	10	L1,L2,L3.

Note 1: Unit 3 and Unit 4 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Understand the architecture and features of microprocessor and microcontrollers..

CO2 Explain the instruction sets of Microcontrollers and write Assembly and High level Programs

CO3 Study the applications of Microcontrollers for real time systems..

CO4 Development of single chip solutions.

CO5 Study the low power 16 bit microcontroller architecture..

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2, PO3

CO2 PO2, PO3

CO3 PO2, PO11, PO12

CO4 PO2, PO3, PO11, PO12

CO5 PO1, PO2, PO3, PO11, PO12

Text Books.

1 Yu-cheng Liu, Glenn A.Gibson, "**Microcomputer Systems: The 8086/8088 Family Architecture, Programming, and Design**", 2005

Kenneth J.Ayala," **The 8051 Microcontroller Architecture, Programming & Applications**",Second Edition, Penram International, 1996/Thomson learning 2005

Muhammad Ali Mazidi, Janice Gillespie Mazidi and Rollin D. McKinlay **"The 8051 Microcontroller and Embedded Systems – using assembly and C",**; PHI, 2006 / Pearson, 2006

John Davies **"MSP430 Microcontroller Basics",** , Elsevier, 2010.

Reference Text Books.

1 Doughlas V. Hall, "Microprocessors and Interfacing Programming and Hardware"

2 "MCS51 Microcontroller family user's manual"

3 "MSP430 Web material"**,** Texas Instruments, 2008.

Subject Title : Control Systems

Sub.Code: EC42 No. of Credits:04=04:00:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 Able to understand the basic concepts of Control systems, types and Transfer Functions.
2 Able to understand the Mathematical models and Analogy of Control Systems and analyze and evaluate the transfer functions using Block Diagram and Signal Flow Graphs.
3 Able to Understand, Analyze, evaluate the Time domain specifications for the second order systems using Step, ramp, impulse and parabolic functions as inputs to the second order systems.
4 Able to Examine and analyze the stability of control systems using time and frequency domain(graphical).
5 Able to understand the concept of state variables and analyze and evaluate the dynamic behaviour of control systems using state variables.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Introduction to Control systems:** Introduction**,** Types of Control systems, Effect of feedback systems and requirements of good control systems: **Mathematical Modeling of Control Systems:** Modeling of mechanical systems (Rotational and Translational excluding Lever and Gear trains systems). Transfer functions (Multivariable systems), Modeling of Electrical systems (Current and voltage analogy) Electromechanical Systems and its Analogous systems and DC Motors (Armature and Field controlled). **Block diagrams:** Block diagram of a closed loop systems and its reduction techniques, Transfer Functions (Multivariable Systems), Applications of Block diagram *TEXT 1.*	11	L1,L2,L3.L4
2	**Signal Flow Graphs:** Mason's gain formula, Basic properties of Signal flow graph, Transfer Functions-(Multivariable systems), Construction of Signal flow graph for closed loop control systems, and Applications of Signal Flow Graphs. **Time Response of feedback control systems:** Time response of control systems**,** Standard test signals, Unit step response of First and Second order Systems. Time response specifications and its derivations, Time response specifications of second order systems, steady state errors and Error constants. Types of control systems(Steady state error for Type 0,1 and 2 systems) *TEXT 1.*	10	L1,L2,L3.
3	**Stability analysis:** Concepts of stability, Necessary conditions for Stability, Routh stability criterion, Difficulties in the formulation of the Routh table, Applications of Routh stability criterion only for linear feedback control systems, Relative stability analysis **Root Locus:** Introduction, Root locus concepts, Construction of Root loci, Rules for the construction of Root-Locus, Determination of roots for a specified open loop gain, Determination of Open loop gain for a	11	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	specified damping of dominant roots, Numerical examples (Only for second order systems) *TEXT 1.*		
4	**Frequency responses analysis:** Introduction, Frequency domain specifications (No derivations, Numerical examples), Correlation between time and frequency response for second order systems. Bode plots, General procedure for constructing the Bode plots(Basic factors), Calculation of transfer function from Magnitude plot, Assessments of relative stability using Bode plots, Computation of Gain and Phase Margins from Bode plot, Gain adjustment in Bode Plot. *TEXT 1.*	12	L1,L2,L3.
5	**State Space Analysis:** Introduction, Concept of State, State variables & State model, State space representation for dynamic systems (Phase variables and Canonical Variables), Solution of state equations(State Transition Matrix(STM) and State transition equation, Properties of STM, Computation of STM by Laplace transformation. Transfer function from the state Model (Electrical networks). *TEXT 1.*	08	L1,L2,L3.

Note 1: Unit 3 and Unit 4 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Ability to Develop and understand the Mathematical Model of Mechanical, Electrical and Electro Mechanical Systems, and also obtain the transfer function by using Block Diagram and Signal Flow Graphs.

CO2 Ability to Analyze and evaluate the first order and second order systems in time domain approach.

CO3 Ability to define, understand, analyze and evaluate the stability of a second order system in Time domain as well as frequency domain specifications.

CO4 Ability to Design and analyze the stability of the second order Control Systems using Root locus, Bode Techniques.

CO5 Ability to use Modern tools to obtain the state models for the electrical and Mechanical systems and evaluate their response in time domain as well as frequency approach.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1, PO2, PO3, PO11, PO12

CO2 PO1, PO2, PO3, PO11, PO12

CO3 PO1, PO2, PO3, PO11, PO12

CO4 PO1, PO2, PO3, PO11, PO12

CO5 PO1, PO2, PO3, PO11, PO12

Text Books.

1 J.Nagarath and M.Gopal, "Control Systems Engineering", 5th Edition, New Age International (P) Limited Publishers, 2005

Reference Text Books.

1 K.Ogata, "Modern Control Engineering", 4th Edition, Pearson Education Asia/PHI, 2002.

2 Benjamin C. Kuo, "Automatic Control Systems" , 9th Edition, John Wiley India Pvt. Ltd., 2008

3 Joseph J Distefano III et al., "Feedback and Control System", 2nd Edition, Schaum's Outlines, TMH, 2007.

Web Links.

1 https://www.electrical4u.com/mathematical-modelling-of-various-system/.

2 https://www.tutorialspoint.com/control_systems/control_systems_time_response_analysis.htm.

3 www.facstaff.bucknell.edu/mastascu/econtrolhtml/rootlocus/rlocus1a.html.

4 lpsa.swarthmore.edu/Bode/BodeExamples.html.

5 https://www.calvin.edu/~pribeiro/courses/engr332/Handouts/nyquist-margins.htm.

6 nptel.ac.in/courses/108103008/25.

Subject Title : Fields and Waves

Sub.Code: EC43 No. of Credits:4=3:2:0 (L - T – P) No. of Lecture Hours/Week : 05
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:65

Course Learning Objectives:

1 Understanding the concepts of vectors, electric fields for EM waves and to analyze and solve problems using coulomb's law, gauss law.
2 Understanding the concepts of energy density, potential difference and capacitance.
3 Understanding the Biot Savart law, Laplace and Poisson's equations and to acquire knowledge of their practical applications.
4 Understanding the importance of Maxwell's equation and applying them for time varying fields.
5 To understand the importance of wave propagation in free space & dielectrics and applying them for time varying fields.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Electrostatics:** Vector analysis, Coulomb's Law and electric field intensity, Field due to continuous volume charge distribution, Field of a line charge. Field of a sheet of charge. Electric flux density, Gauss' law and its applications. Divergence, Maxwell's First equation (Electrostatics), vector operator ∇ and divergence theorem **TEXT 1**	13	L1,L2,L3.
2	**Energy and potential:** Energy expended in moving a point charge in an electric field, The line integral, Definition of potential difference and Potential, The potential field of a point charge and system of charges, Potential gradient , Energy density in an electrostatic field. **C**apacitance and examples. **TEXT 1**	12	L1,L2,L3.
3	**Poisson's and Laplace's equations:** Derivations of Poisson's and Laplace's Equations, Uniqueness theorem, Examples of the solutions of Laplace's and Poisson's equations. **Magnatostatics:** The steady magnetic field - Biot-Savart law and its applications, Ampere's circuital law and its applications, magnetic flux and flux density, scalar and Vector magnetic potentials. Magnetic forces - Force on a moving charge and differential current element, Force between differential current elements. **TEXT 1**	14	L1,L2,L3.
4	**Maxwell's equations:** Inductance and examples, Faraday's law, Displacement current. Maxwell's equation in point and Integral form, Boundary conditions for perfect dielectric materials, magnetic boundary conditions. **TEXT 1**	13	L1,L2,L3.
5	**Electromagnetic waves:** Wave propagation in free space and dielectrics, Poynting's theorem. Propagation in good conductors – skin effect. Wave polarization. Reflection of uniform plane waves at normal incidence, standing wave ratio. **TEXT 1**	13	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.

Note 1: Unit 3 and Unit 5 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Ability to apply the concepts of vectors, electric fields for EM waves and to analyze and solve problems using coulomb's law, gauss law.

CO2 Ability to apply the concepts of energy density, potential difference and capacitance.

CO3 To analyze Biot Savart law, Laplace and Poisson's equations and to acquire knowledge of their practical applications.

CO4 To emphasize the importance of Maxwell's equation and applying them for time varying fields.

CO5 To emphasize the importance of wave propagation in free space & dielectrics and applying them for time varying fields.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO5,PO6

CO2 PO1,PO2,PO5,PO6

CO3 PO1,PO2,PO5,PO6

CO4 PO1,PO2,PO5,PO6

CO5 PO1,PO2, PO5,PO6,P11,P12

Text Books.

1 William H Hayt Jr. and John A Buck, "**Engineering Electromagnetics**", 8th edition, McGraw-Hill, **2012**

2 David K Cheng, "**Field and Wave Electromagnetics**", 2nd edition, Pearson Education Asia, Indian Reprint – 2001

Reference Text Books.

1 John Krauss and Daniel A Fleisch , "**Electromagnetics with Applications**", 5th edition, McGraw-Hill, **1999**

2 Edward C. Jordan and Keith G Balmain,, "**Electromagnetic Waves and Radiating Systems**", 2nd Edition, Prentice – Hall of India / Pearson Education, Reprint – ***2002***

Web Links.

1 www.google.com , david k cheng fields and waves electromagnetics pdf download

2 www.google.com, william h hayt engineering electromagnetics pdf

3 www.nptelcoursematerials

4 ncptel.ac.in/lectures/108108073

5 www.youtube/electromagnaticsforengineers

Sub Title : Verilog HDL		
Sub Code:EC44	**No. of Credits:4=4 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : 3 Hours	**CIE +Assignment + SEE = 45 + 05 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. Describing the EDA flow of digital design and recognizing the importance of HDL.
2. Able to design and analyze the digital circuits using dataflow and gate level modeling.
3. Implementation of digital circuits at behavioral level.
4. Understand the concepts of tasks and functions.
5. To gain the knowledge on synthesis of digital design and understanding the various logic devices available for the synthesis.

UNIT No	Syllabus Content	No of Hours
1	**Overview of digital design with Verilog HDL:** Evolution of Computer Aided Digital Design, Emergence of HDLs, Typical Design flow, Importance of HDLs, Popularity of Verilog HDL, Trends in HDLs. **Basic Concepts:** Lexical conversions, Data types, System tasks and Compiler directives. **Text-1**	10
2	**Modules and ports:** Modules, Ports, Hierarchical Names. **Gate Level Modeling:** Gate types, Gate delays. **Data Flow Modeling**: Continuous assignments, Delays, Expressions, Operators, and operands, operator types, Examples. **Text-1**	11
3	**Behavioral Modeling:** Structured Procedures, Procedural Assignments, Timing controls, Conditional statements, Multiway branching, Loops, Sequential and Parallel Blocks, Generate blocks, Examples. **Text-1**	10
4	**Tasks and functions:** Difference between Tasks and Functions, Tasks, Functions. **Modeling Examples:** Modeling simple elements, Different styles of modeling, Modeling Delays, Modeling a Truth Table, Modeling Conditional Operations, Modeling Synchronous Logic, Generic Shift Register, State Machine Modeling, Interacting State Machines, Modeling a Moore FSM, Modeling a Mealy FSM. **Text-1 & Text-2**	10
5	**Logic synthesis with Verilog HDL**: What is Logic synthesis, Impact of Logic Synthesis, Verilog HDL synthesis, Synthesis Design Flow, Verification of Gate Level Netlist. Programmable Logic Devices: PLA, PAL, Programming of PLA and PAL, CPLDs, FPGA, Applications of CPLDs and FPGAs. **Text-1 & Text-3**	11

Note 1. Unit 4 and Unit 5 will have internal choice.

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2. Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1. Understand the HDL design flow and lexical conventions of the language.
CO2. Ability to design combinational and sequential circuits in different styles.
CO3. Able to design and test the circuits using behavioral modeling.
CO4. Ability to design the circuits using the subroutines and to model FSM in Verilog.
CO5. Ability to understand the concept of synthesis and programmable logic device.

Cos	Mapping with POs
CO1	PO2,PO3
CO2	PO2,PO3
CO3	PO2,PO3
CO4	PO2,PO3
CO5	PO2,PO3,PO4

TEXT BOOKS:

1. Samir Palnitkar, **"Verilog HDL – A guide to Digital Design and Synthesis",** Pearson, 2003.
2. J. Bhasker," **A verilog HDL Primer**" BS Publications , 2nd Edition.
3. Stephen Brown, ZvonkoVransic," **Fundamentals of digital logic with verilog Design**", TMH,2 nd Edition.

REFERENCE BOOKS/WEB LINKS:

1. Charles H. Roth, "**Digital Systems Design Using VHDL**", Thomson Learning, Inc, 1st Edition, 2002.
2. D Perry, "**Introduction to VHDL programming**", 4th Edition ,2002
3. Floyd, " **Digital Fundamentals using VHDL**", Pearson Education, 2nd Edition, 2003

Subject Title : Linear integrated circuits

Sub.Code: EC45 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 TO understand the working of basic OPAMP circuit as amplifiers
2 Analysis of various circuits as rectifiers, clippers, differentiator, integrator using Op-amps
3 To Study the concept of 555 timer as astable and monostable multivibrator
4 Design of Low pass & high pass filters, oscillators and to study the frequency response of op-amps
5 Study the concept of voltage regulators, ADC and DAC

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Brief review of Op-amps.** **Op-Amps as AC Amplifiers:** Capacitor coupled Voltage Follower, High Zin-Capacitor coupled Voltage follower, Capacitor coupled Non-inverting Amplifier, High Zin Capacitor coupled Non-inverting Amplifier, capacitor coupled inverting amplifier. **TEXT-1**	10	L1,L2,L3.
2	**Signal Processing Circuits:** Non Saturating precision HWR rectifier ,Precision full wave rectifier : HWR and summing circuit , high input impedance precision FWR , Limiting circuits : peak clipper , Dead zone circuit , Precision clipping circuit , Precision Clamping circuit , Sample and Hold circuit. **Switching, Differentiating and integrating circuits:** Op-amps in switching Circuits, Voltage level detectors. Inverting Schmitt trigger circuit using Op-amps. Differentiating circuits: differentiating circuit waveforms, basic differentiating circuit, Integrating circuit: Integrating circuit waveforms, basic integrating circuit. **TEXT-1**.	11	L1,L2,L3.
3	**Signal Generators:** Astable multivibrator, Mono stable Multivibrator , Triangular wave generator. 555 timer, monostable multivibrator using 555 timer, (No derivation), 555 astable multivibrator. Opamp linear Applications: Voltage sources, current sources and sinks, current amplifiers. **TEXT-1**	09	L1,L2,L3.
4	**Op-Amp frequency response and compensation**: Circuit stability, Frequency compensation methods, internally compensated OP-amps. Circuit stability precautions. **Sinusoidal Oscillators:** Phase shift and quadrature oscillators, Colpits and Hartley Oscillators, Oscillator amplitude stabilization. **Active Filters:** Filter types and characteristics, First order Active	11	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	LP and HP filters, Second order filters, Band pass filters, notch filters. All pass phase shifting characteristics. **TEXT-1**		
5	**DC Voltage Regulators:** Voltage regulator basics, OP-amps series voltage regulator, Adjustable output voltage regulator, IC linear voltage regulator (723IC). **DAC , ADC:** Analog/ Digital conversion basics , DAC – Weighted resister DAC , R to 2R DAC , ADC – parallel ADC , ADC counting methods – linear ramp, successive approximation ADC. **TEXT-1**.	11	L1,L2,L3.

Note 1: Unit 4 and Unit 5 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Outline basics of opamp and analyze opamp as amplifiers

CO2 Analysis of opamp as signal processing circuits, switching, differentiating and integrating circuits.

CO3 Understanding opamp as astable and monostable multivibrator.

CO4 Design of filters & oscillators circuit.

CO5 Basics of data converter, and voltage regulator.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2,PO3,PO6

CO2 PO2,PO3,PO6

CO3 PO2,PO3, PO6

CO4 PO2,PO3,PO6

CO5 PO2,PO3,PO6

Text Books.

1 David A. Bell, "**Operational Amplifiers and Linear IC's**", Third Edition, Oxford HE, 2011

Reference Text Books.

1 D. Roy Choudhary and Shail B. Jain, "Linear Integrated Circuits", 3rd edition, publisher, 2007

Sub Title : MICROCONTROLLER LAB		
Sub Code:ECL46	**No. of Credits:1=0 : 0 : 1 (L-T-P)**	**No. of lecture hours/week : 02**
Exam Duration : 03 Hours	**CIE +Assignment + SEE = 50 + 50 =100**	**Total No. of Contact Hours : 26**

Course objectives:

1. To learn the architecture of 8051 Microcontroller.
2. To learn the Instruction set and Embedded C for MCS51.
3. Ability to write a ALP and C program for a given algorithm and implement the same
4. To learn the I/O ports and interfacing techniques with MCS51.
5. Ability to develop single chip solution using MCS51.

Unit No.	Syllabus contents	No of Hours
PART-A	**PROGRAMMING WITH 8051 MICROCONTROLLER**	
1.	**Data Transfer**: Block move, Exchange, Finding largest element in an array, sorting.	2
2.	**Arithmetic Instructions**: Addition/subtraction, multiplication and division, square, Cube	3
3.	**Counters:** 8/16 bit (Software)	2
4.	**Boolean & Logical Instructions (Bit manipulations):** Logic gates, Adder/Subtractor, multiplexer circuits	2
5.	**Code conversion**: BCD – ASCII; ASCII – Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX.	2
6.	**Programs to generate time delay using** on-Chip timer/Counter, Program as event counter, Programs using serial port and Programs using interrupts.	2
PART B	**INTERFACING PROGRAMS: Write C programs to interface 8051** to interfacing modules to develop single chip solutions.	
7.	Key board and Alphanumeric LCD panel input interface to 8051	2
8.	External ADC and Temperature control interface to 8051.	2
9.	Generation of waveforms: Sine, Square, Triangular, Ramp etc. using DAC interface (change the frequency and amplitude)	4
10.	Stepper and DC motor control interface to 8051	2

Course Outcomes:

CO1. Understand the architectural features of microcontrollers.
CO2. Explain the instruction sets of Microcontrollers and write Assembly and High level Programs.
CO3. Study the various features of Microcontrollers based systems.
CO4. Study the applications of Microcontrollers for real time systems.
CO5. Development of single chip solutions.

Cos	Mapping with POs
CO1	PO2, PO3
CO2	PO2, PO3
CO3	PO2, PO3, PO11, PO12
CO4	PO2, PO3, PO11, PO12
CO5	PO2, PO3, PO11, PO12

TEXT BOOK:

1. **"The 8051 Microcontroller Architecture, Programming & Applications",** 2e Kenneth J. Ayala, Penram International, 1996 / Thomson Learning 2005.
2. **"The 8051 Microcontroller and Embedded Systems – using assembly and C",** Muhammad Ali Mazidi, Janice Gillespie Mazidi and Rollin D. McKinlay; PHI, 2006 / Pearson, 2006

Sub Title : HDL LAB		
Sub Code:ECL47	**No of Credits : 0:0:1:0(L:T:P)**	**No of lecture hours/week : 02**
Exam Duration : 03 Hours	**CIE +Assignment + SEE = 50 + 50 =100**	**Total No. of Contact Hours :26**

Course objectives:

1. Acquire skills to develop programs for digital design.
2. Verify the designs by simulation tools such as Altera/Xilinx.
3. To synthesize the designs on FPGA/CPLDs.
4. To interface different modules to FPGA.

Unit No.	Syllabus contents	No of Hours
1	Write the Verilog code and its test bench to realize all the logic gates.	2
2	Write the Verilog code with test bench to simulate the following combinational designs. a. 2 to 4 decoder b. 8 to 3 (encoder without priority & with priority) c. 8 to 1 multiplexer d. 4 bit binary to gray converter e. Multiplexer f. de-multiplexer g. Comparator	3
3	Write the Verilog code and its test bench to realize the functions of a Full Adder using all modeling styles.	2
4	Write the hardware description code and test benchfor 4-bit ALU. An ALU is a hardware that can give the result of various arithmetic and logical operations of the two numbers based on a control signal.	2
5	Write the Verilog code and its test bench for the SR, D, JK and T flip-flops.	2
6	Design and develop the Verilog code for 4 bit - binary counter, Synchronous, Asynchronous and Ring counter.	3
7	Write the Verilog code for 8-bit register with shift left and shift right modes of operation and test its operation.	2
8	Write a program to illustrate the function and tasks.	2
PART B	**Interfacing Programs.**	
9	Write the Verilog code to control external light using relay.	2
10	Write Verilog code to generate different waveforms (Sine, Square, Triangle and Ramp) vary the frequency and amplitude using DAC.	2
11	Write the Verilog code to interface the stepper motor and vary the speed and direction.	2
12	Write a program to implement keypad interface.	2

Course Outcomes:

CO1. Design, Simulation and synthesis of various digital circuits.
CO2. Waveforms generation using FPGA.
CO3. Interfacing motor and hex keypad on FPAGA.

Cos	Mapping with POs
CO1	PO2,PO3
CO2	PO2,PO3
CO3	PO2,PO3
CO4	PO2,PO3
CO5	PO2,PO3,PO4

TEXT BOOKS:

1. Samir Palnitkar, **"Verilog HDL – A guide to Digital Design and Synthesis",** Pearson, 2003.
2. J. Bhasker," **A verilog HDL Primer**" BS Publications , 2nd Edition.
3. Stephen Brown, ZvonkoVransic," **Fundamentals of digital logic with verilog Design**", TMH,2 nd Edition.

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2. D Perry, "**Introduction to VHDL programming**", 4th Edition ,2002
3. Floyd, " **Digital Fundamentals using VHDL**", Pearson Education, 2nd Edition, 2003

(EFFECTIVE FROM ACADEMIC YEAR 2017-18)

Scheme of Teaching for V Semester B.E (2015 Batch)

Subject Code	Title	Teaching Dept.	Contact hours/week				Examination		
			Theory	Tutorial	Practical	No of credits	CIE	SEE	Total Marks
EC51	Microwave Engineering	EC	03	00	00	03	50	50	100
EC52	Digital Signal Processing	EC	04	00	00	04	50	50	100
EC53	Analog Communication	EC	03	00	00	03	50	50	100
EC54	Fundamentals of CMOS VLSI	EC	04	00	00	04	50	50	100
EC55	Antenna and Wave Propagation	EC	04	00	00	04	50	50	100
EC56	Object Oriented Programming with C++	EC	04	00	00	04	50	50	100
ECL57	DSP Lab	EC	00	00	03	1.5	50	50	100
ECL58	Analog Communication Lab	EC	00	00	03	1.5	50	50	100
TOTAL			**22**	**00**	**06**	**25**	**400**	**400**	**800**

CHAIRMAN BOS **DEAN (ACADEMIC)** **PRINCIPAL**

((EFFECTIVE FROM ACADEMIC YEAR 2017-18)

Scheme of Teaching for VI Semester B.E (2015 Batch)

Subject Code	Title	Teaching Dept.	Contact hours/week				Examination		
			Theory	Tutorial	Practical	No of credits	CIE	SEE	Total Marks
HS03	Management & Entrepreneurship	MBA	04	00	00	04	50	50	100
EC61	Analog and Mixed Mode VLSI	EC	03	00	00	03	50	50	100
EC62	Digital Communication	EC	04	00	00	04	50	50	100
EC63	Embedded System Design	EC	03	00	00	03	50	50	100
EC64	Information Theory and Coding	EC	03	00	00	03	50	50	100
EC65X	ELECTIVE_1 (GROUP-A)	EC	04	00	00	04	50	50	100
ECL66	Advanced Communication Lab	EC	00	00	03	1.5	50	50	100
ECL67	Embedded System Lab	EC	00	00	03	1.5	50	50	100
ECP68	Mini-Project	EC	00	00	03	02	50	50	100
TOTAL			**21**	**00**	**9**	**26**	**450**	**450**	**900**

SUBJECT CODE	**ELECTIVE -1 (Group A) Credits-4**
15EC651	Artificial Neural Network
15EC652	Adaptive Signal Processing
15EC653	Digital Switching Systems
15EC654	Power Electronics

CHAIRMAN BOS **DEAN (ACADEMIC)** **PRINCIPAL**

Sub Title : Microwave Engineering		
Sub Code: EC51	**No. of Credits: 3= 3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : **3 Hours**	**CIE +Assignment + SEE =** **45 + 05 + 50 =100**	**Total No. of Contact Hours : 39**

Course objectives:

1. To gain the knowledge of Transmission line theory.
2. To interpret the knowledge of Electromagnetic fields in wave guides.
3. To analyze the Microwave junctions and power flow across them.
4. To gain the knowledge of microwave diodes, and tubes.
5. To interpret the knowledge of transmission line theory in strip lines.

UNIT No	Syllabus Contents	No of Hours
1	**Microwave Transmission Lines**: Introduction, Transmission Line Equations and Solutions: Transmission-Line Equations, Solutions of Transmission Line Equations. Reflection Coefficient and Transmission Coefficient. Standing Wave and Standing-Wave Ratio. Line Impedance and Admittance. Text 1	08
2	**Microwave waveguides and components:** Introduction, rectangular waveguides: Properties and characteristics of wave guides, solution of wave equations in rectangular coordinates, TM modes in rectangular waveguides, TE modes in rectangular waveguides, field patterns of TM_{11} and TE_{10} waves. Excitation of modes in rectangular wave guide. **Circular waveguides:** solution of wave equation in cylindrical coordinates, TM and TE modes in circular wave guides (No derivations), cut off frequency, cut off wavelength, dominant mode, field patterns for dominant modes, Numerical problems. Text 1	10
3	**Microwave Hybrid circuits and passive devices:** Introduction, S matrix representation of multiport network, properties of S-matrix (No derivation). Waveguide Tees: H plane and E plane T, E-H plane or magic T, Directional coupler: Bethe hole and Two hole directional coupler: Directivity, coupling factor, Isolation. Text 1	07
4	**Solid state microwave devices and tubes:** PIN diode, TED – introduction, GUNN effect diodes, RWH theory, modes of operation. ATTD devices – introduction, Read diode, IMPATT and TRAPATT diodes. **Microwave tubes** –introduction, Klystrons: Two cavity Klystron, velocity modulation process, bunching process, Reflex Klystron-operating characteristics. Text 1	07
5	**Microwave passive devices:** Phase shifters, attenuators, Ferrite devices – Faraday rotation in Ferrites, Isolator and circulator. **Strip lines:** Strip lines, micro strip lines, and types of micro strip lines (qualitative analysis only). Text 1	07

Note 1: Unit 2 and Unit 4 will have internal choice.

Note 2:Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2.

Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1.	Gain the knowledge of Transmission line theory.
CO2.	Apply the knowledge of Electromagnetic fields in wave guides.
CO3.	Analyze the different Microwave junctions and power flow across them.
CO4.	Understand the functioning of microwave diodes, and tubes.
CO5.	Interpret the knowledge of transmission line theory in strip lines and describe the functioning of different microwave passive devices.

Cos	Mapping with POs
CO1	PO1,PO2,PO12
CO2	PO1,PO2
CO3	PO1,PO4
CO4	PO1,PO12
CO5	PO6,PO12

TEXT BOOK:

1. Samuel Y. Liao, "**Microwave Devices and circuits"**, Pearson Education, 3rd edition 2005.
2. Devid M. Pozar– **"Microwave Engineering"**, John Wiley & sons, Inc., 4th edition 2011

REFERENCE BOOKS / WEBLINKS:

1. Annapurna Das, Sisir K Das**, "Microwave Engineering ",** TMH publications, 2005.
2. M. Kulkarni,**"Microwave and Radar engineering",** Umesh publications, New Delhi.
3. Robert Collin, **"Foundations for Microwave engineering ",** Wiley Publications, 2nd Edition- 2013.

Subject Title : Digital Signal Processing

Sub.Code: EC52 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 To gain the knowledge of the sampling process, frequency domain response of LTI systems, invertible systems, Discrete Fourier Transforms, Fast Fourier Transforms, IIR and FIR filters and their structures
2 To interpret the sampling process, Frequency domain response of LTI systems, Inverse Systems, DFT and their properties, FFT algorithms and IIR and FIR filters
3 To apply the concept of sampling theorem, Frequency domain response of LTI systems, DFT, FFT algorithms and IIR and FIR filters
4 To illustrate the Frequency domain response of LTI systems, DFT, FFT algorithms and IIR and FIR filters
5 To design the analog IIR, digital IIR and FIR filters

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Sampling theorem, Frequency domain characteristics of LTI systems and Inverse systems:** Analog to digital conversion, Sampling of analog signals, Sampling theorem, Response to complex exponential and sinusoidal signals, Relationship between the system function and the frequency response function. Inverse systems and deconvolution, Invertibility of LTI systems, minimum phase, maximum phase and mixed phase systems. TEXT 1 and TEXT 2	10	L1,L2,L3.
2	**Discrete Fourier Transform (DFT):** Frequency domain sampling and reconstruction of discrete time signals. DFT as a linear transformation, Properties of DFT: Periodicity, linearity, Symmetry properties, Circular folding, Circular Convolution, Circular time shift, Circular frequency shift, Complex conjugate property, Multiplication of two sequences, Use of DFT in linear filtering, overlap-save and overlap-add method. TEXT 1 and TEXT 2	11	L2,L3,L4,L5
3	**Fast-Fourier-Transform (FFT) Algorithms:** Direct computation of DFT, need for efficient computation of the DFT (FFT algorithms). Radix-2 FFT algorithm for the computation of DFT and IDFT: Decimation-in-time (DIT) and Decimation-in-frequency (DIF) algorithms. TEXT 1	12	L2,L3,L4,L5
4	**IIR Filter Design:** Characteristics of commonly used analog filters – Butterworth and Chebyshev filters, analog to analog frequency transformation. **Design of IIR Digital filters from analog filters (Butterworth and Chebyshev Type):** Impulse Invariance method and Bilinear transformation method, Derivation and design problems.	10	L3,L4,L5,L6

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	TEXT 1		
5	**FIR Filter Design:** Introduction to FIR filters, Design of FIR filters using Rectangular, Hamming and Hanning windows. **Implementation of Discrete-Time Systems:** Structures for IIR systems: Direct form I & II, Cascade & Parallel form realization. Structures for FIR systems: Direct form, Linear phase, Cascade form. **Introduction to Multirate Digital Signal Processing:** Introduction, Decimation by factor D, Interpolation by factor I. TEXT 1 and TEXT 2	11	L3,L4,L5,L6

Note 1: Unit 2 and Unit 4 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Define the sampling process, frequency domain response of LTI systems, invertible systems, Discrete Fourier Transforms, Fast Fourier Transforms, IIR and FIR filters and their structures

CO2 Understand sampling process, Frequency domain response of LTI systems, Inverse Systems, DFT and their properties, FFT algorithms and IIR and FIR filters.

CO3 Demonstrate the application of sampling theorem, Frequency domain response of LTI systems, DFT, FFT algorithms and IIR and FIR filters.

CO4 Analyze the Frequency domain response of LTI systems, DFT, FFT algorithms and IIR and FIR filters.

CO5 Design the analog IIR, digital IIR and FIR filters.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1, PO2, PO5

CO2 PO1, PO2, PO5

CO3 PO1, PO2, PO5

CO4 PO1, PO2, PO5

CO5 PO1, PO2, PO5

Text Books.

1 Proakis & Monalakis, "Digital Signal Processing-Principles Algorithms & Applications", Fourth Edition, Pearson Education, New Delhi, 2009

2 Emmanuel Ifeachor and Barrie Jervis, "Digital Signal Processing: A Practical Approach", 2nd edition, Pearson Education, New Delhi, 2002

Reference Text Books.

1 Alan V. Oppenheim and Schaffer, "Discrete Time Signal Processing", 2nd edition, PHI, 2007

2 Sanjit K. Mitra, "Digital Signal Processing", 3rd edition, Tata Mc-Graw Hill, 2010

3 Lee Tan, "Digital Signal Processing", edition, Elsevier publications, 2007

4 Shenoy, "Introduction to Digital Signal Processing and Filter Design", 1st edition, John Wiley & Sons, 2010

5 Lonnie C. Ludeman, "Fundamentals of Digital Signal Processing", International edition, John Wiley & Sons, 1988

Web Links.

1 http://nptel.ac.in/courses/117102060/

2 https://ocw.mit.edu/resources/res-6-008-digital-signal-processing-spring-2011/study-materials/

Subject Title : Analog Communication

Sub.Code: EC53 No. of Credits:03=03:0:0 (L - T – P) No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:39

Course Learning Objectives:

1 Understand and Analyse the Communication basic concepts and modulation Process.
2 Analyse and compare the Modulation techniques and its applications.
3 Analyse and Implement Angle Modulation Techniques.
4 Analyse, Compare and understand types of noise in communication systems.
5 Analyse and understand the noise intervention in modulation techniques.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Introduction:** Block diagram of communication system, Rayleigh energy theorem, Hilbert transform, pre-envelope, canonical representation of band pass signals, band pass systems, phase and group delay. **Continuous Wave Modulation:** Introduction, Amplitude modulation, Generation of AM wave: switching modulator, Detection of AM waves: envelop detector, virtues and limitations and modifications of AM TEXT 1	07	L1,L2,L3.
2	**Double side band suppressed carrier modulation (DSBSC):** Generation of DSBSC: Ring modulator, Coherent detection of DSBSC, COSTAS Receiver, Quadrature–carrier multiplexing, Numerical examples. **Vestigial Side-Band Modulation (VSB):** Television signals, waveform distortion. **Single Side-Band Modulation (SSB):** Time-Domain description, Demodulation of SSB signals. Frequency translation, Frequency Division Multiplexing (FDM). **Applications**: Radio broadcasting, AM radio, Numerical examples. TEXT 1	09	L1,L2,L3.
3	**Angle Modulation:** Frequency Modulation: Narrow band Frequency modulation, wide band FM, transmission band width of FM waves, generation of FM waves: indirect FM and direct FM. Demodulation of FM waves, FM stereo multiplexing, Phase-locked loop (PLL), Numerical examples. TEXT 1	07	L2,L3,L4
4	**Random Process:** Random variables: Several random variables. Statistical averages: Function of Random variables, moments, Mean, Correlation and Covariance function: Principles of autocorrelation function, Cross – correlation functions, Numerical examples. **Noise:** Introduction, shot noise, thermal noise, white noise, Noise	09	L2,L3,L4

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	equivalent bandwidth, Narrow band noise, sine wave plus narrowband noise. Noise Figure, Equivalent noise temperature, and cascade connection of two-port networks. Numerical examples. TEXT 1		
5	**Noise in Continuous Wave Modulation Systems:** Introduction, Receiver model, Noise in DSB-SC receivers, Noise in SSB receivers, Noise in AM receivers, Threshold effect, Noise in FM receivers, FM threshold effect, Numerical examples. TEXT 1	07	L2,L3,L4

Note 1: Unit 2 and Unit 4 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 To learn the basic block diagram of communication systems and Modulation schemes.

CO2 Ability to understand the DSBSC and SSB modulation and demodulation technique.

CO3 Ability to understand Angle modulation and demodulation techniques in terms of mathematical models.

CO4 Ability to understand Random Signal in communication systems and noise basics.

CO5 Analysis of Noise effect in modulation schemes in communication system.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2, PO3

CO2 PO4, PO5

CO3 PO4, PO5

CO4 PO6, PO12

CO5 PO6, PO12

Text Books.

1 Simon Haykins, “Communication systems”, Third Edition, John Willey, 1996.

2 Simon Haykins, “An Introduction to Analog and Digital Communication”, John Wiley, 2003.

Reference Text Books.

1 B P Lathi, “Modern Digital and Analog Communication Systems”, Third edition, Oxford University Press, 2005.

2 Singh and Sapre, “Analog and Digital Communication Systems”, Second edition, TMH, 2007.

3 John G Proakis and Masood Saleh, “Communication Systems Engineering”, Second edition, Prentice Hall, 2001.

Web Links.

1 http://www.nptelvideos.in

Subject Title : Fundamentals of CMOS VLSI

Sub.Code: EC54 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 To become familiar with the Basic of MOS technologies.
2 Study the basics of device equations
3 Understand different CMOS logic structures
4 To analyse adder circuits
5 To analyse multiplier circuits

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Basic MOS Technology:** Integrated circuits era, Enhancement and Depletion mode MOS transistors, CMOS fabrication, BiCMOS technology. **MOS Transistor Theory:** Introduction, MOS Device Design Equations, the Complementary CMOS Inverter – DC Characteristics, Static Load MOS Inverters, the Transmission Gate, Tristate Inverter. **Circuit Design Processes:** MOS layers, Stick diagrams, Design rules and layout – lambda-based design rules, Examples, Layout diagrams, Symbolic diagrams. Basic Physical Design of Simple logic gates. TEXT 1 and TEXT 2	12	L1,L2,L3.
2	**Basic Circuit Concepts:** Sheet resistance, Area capacitances, Capacitance calculations, The delay unit, Inverter delays, Driving capacitive loads, Propagation delays. **Scaling of MOS Circuits:** Scaling models and scaling factors, Scaling factors for device parameters, Limitations of scaling TEXT 1	10	L1,L2,L3.
3	**CMOS Logic Structures:** CMOS Complementary Logic, Bi CMOS Logic, Pseudo-nMOS Logic, Dynamic CMOS Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS Domino Logic Cascaded Voltage Switch Logic (CVSL). TEXT 1 and TEXT 2	09	L1,L2,L3.
4	**Data Path Subsystems I:**Introduction, addition/subtraction, single bit addition, carry propagate addition, carry ripple adder, carry generation & propagation, Manchester carry chain adder, carry skip adder, carry look ahead adder, carry select, carry increment ,conditional sum adders, adder variants. TEXT 1 and TEXT 3	11	L1,L2,L3.
5	**Data Path Subsystems II:** Multiplication, unsigned array multiplication, 2's complement array multiplication, Booth encoding, Wallace tree multiplication, Serial multiplication.	10	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	TEXT 1 and TEXT 3		

Note 1: Unit **1** and Unit **4** will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Outline the basics of VLSI technology

CO2 Explanation of circuit design process and MOS transistor theory..

CO3 Analysis of component parameters.

CO4 Describe different logic structures.

CO5 Design of Arithmetic circuits using MOS transistors.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2,PO3,PO6,PO7

CO2 PO2,PO3,PO6,PO7

CO3 PO2,PO3,PO6,PO7

CO4 PO2,PO3,PO6,PO7

CO5 PO2,PO3,PO6,PO7

Text Books.

1 Douglas A. Pucknell& Kamran Eshraghian, "**Basic VLSI Design**", Third Edition, PHI, 2005

2 Neil H. E. Weste, K. Eshragian, "**Principles of CMOS VLSI Design - A Systems Perspective**", Second edition, Pearson Education (Asia) Pvt. Ltd, year

3 Neil H.E Weste, David Harris, Ayan Banerjee, "**CMOS VLSI design- A circuits and systems perspective**", Third edition Pearson Education (Asia) Pvt. Ltd, 2006

Reference Text Books.

1 R. Jacob Baker, "**CMOS Circuit Design, Layout and Simulation**", edition, John Wiley India Pvt. Ltd, year

2 Sung- Mo Kang & Yusuf Leblebici, "**CMOS Digital Integrated Circuits: Analysis and Design**", Third edition, Tata McGraw-Hill Publishing Company Ltd, 2007

Web Links.

1 www.nptel.com

Subject Title: ANTENNA AND WAVE PROPAGATION

Sub.Code: EC55 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 Describe the fundamental parameters of the antenna.
2 Describe the radiation from electric dipole.
3 Describe the operation of array of antennas and their radiation patterns.
4 Explain the different types of antennas used in LF and VHF.
5 Explain the frequency independent antennas and different modes of wave propagation in free space.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Antenna Terminology** : Introduction, Isotropic radiators, Radiation pattern, radiation intensity, Gain – Directive gain, power gain, Directivity, antenna efficiency, effective area , effective height , transmission between two antennas, radiation resistance , antenna beam width , beam efficiency, polarization, antenna temperatures, Numerical. **Text Book: 1 & 2**	08	L1, L2 , L3.
2	**Electric Dipoles and Thin Linear Antennas:** Introduction, short electric dipole, Retarded vector potential, fields of a short dipole, radiation resistance of short dipole, radiation from a half wave dipole (power radiation and radiation resistance), linear antenna and its effective length, Numerical. **Text Book: 1 & 2**	10	L1, L2, L3.
3	**Point Sources and Arrays**: Introduction, point sources, power patterns, filed patterns, phase patterns, power theorem, radiation intensity and examples. Various forms of antenna array, Array of two isotropic point sources, Non-isotropic but similar point sources, Multiplication of pattern and examples, linear array with n isotropic point sources of equal amplitude and spacing and examples, non-isotropic point sources, broad side array and end fire with non-unipolar amplitude distribution, Binomial arrays. **Text Book: 1 & 2**	11	L1, L2, L4.
4	**Practical Antennas:** Low frequency antennas – The V antenna, Rhombic antenna and design of rhombic antenna , Loop antenna- EMF Equation of loop antenna, errors in loop direction finding, radiation resistance and directivity of loop antenna, examples. VHF antennas –folded dipole antenna, Yagi-Uda antenna, voltage and	11	L2, L3, L5.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	current relations in Yagi-uda antenna, Horn antenna and examples, Babbinet's principle and complementary antennas, micro strip antenna, Introduction microwave antenna. **Text Book: 2**		
5	**Frequency Independent Antennas and Introduction to Wave Propagation:** condition for frequency independence, frequency independent of conical-spiral antenna, frequency independent of log-periodic (dipole array) antenna, design of log periodic dipole antenna **Introduction To Propagation:** Modes of propagations-ground wave, sky wave, space wave and tropospheric scatter propagation. Structure of atmosphere. Characteristics of different ionized regions. Sky Wave Propagation, Definitions- Virtual Height, Maximum Usable frequency, Skip distance, Space wave propagation, Duct Propagation, Numerical **Text Book: 2**	12	L2, L3, L5.

Note 1: **Unit 4 and Unit 5 will have internal choice.**

Note 2: **Two assignments are evaluated for 5 marks: Assignment – 1 from units 1, 2 and 3. Assignment - 2 from unit 4 and 5.**

Course Outcomes:

CO1 Describe and identify different types of antennas and list modes of wave propagation.

CO2 Explain the working and characteristics of each type of antenna and modes of wave propagation

CO3 Draw and illustrate antenna patterns, Design antennas for the given specifications.

CO4 Examine the parameters of antenna and derive radiation resistance of electric dipole of antenna.

CO5 Evaluate the radiation patterns and radiation intensity of antenna.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1, PO2,PO12

CO2 PO1, PO2,PO12

CO3 PO1,PO2,PO4

CO4 PO1, PO2,PO3,PO5,PO12

CO5	PO2, PO5,PO12

Text Books.

1. John D Kraus, Ahmad S Khan, "ANTENNAS AND WAVE PROPAGATION", Forth Edition, Tata McGraw-Hill International, 2010
2. K D Prasad, "ANTENNA & WAVE PROPAGATION", Satya Prakashan,New Delhi, 3rd edition, 2012
3. A Balanis,"Antenna Theory- Analysis and Design",3rd edition, John Wiley Interscience Publication,2004

Reference Text Books.

1. A R. Harish , M. Sachidananda," ANTENNA AND WAVE PROPAGATION", Oxford University Press,2007
2. U A Bakshi, A V Bakshi,"Antenna and Wave Propagation ", Technical Publication
3. G S N Raju," Antenna and Wave Propagation", PEARSON Publication, 2012

Web Links.

1. http://www.rfwireless-world.com
2. https://www.accessengineeringlibrary.com/browse/practical-antenna-handbook-fifth-edition
3. https://www.audiolinks.com
4. http://www.radio-electronics.com/info/propagation/radio-propagation/radio-propagation-overview-tutorial.php

Subject Title : Object Oriented Programming with C++

Sub.Code: EC56 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:04 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:62

Course Learning Objectives:

1. Listing OOPs concepts and recognizing the programming elements.
2. Developing and managing the object oriented programs.
3. Understanding the concepts of OOPS to develop the robust programs.
4. Understand and manage the error handling.
5. Concepts of file operations.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Beginning with C++-**Basic concepts of object oriented programming, structure of C++ program, basic data types, user defined data types, derived data types, reference variables, operators in C++, scope resolution operator, memory management operators, manipulators, implicit conversions and control structures. **Functions in C++:** The main function, function prototyping, call by reference, return by reference, inline function, default arguments, const arguments, recursion, function overloading, Friend and virtual Functions. TEXT-1 Click here to enter text.	10	L1,L2,L3.
2	**Classes and Objects*:*** C structures revisited, Specifying a class, Defining member function, A C++ program with class, making outside function inline, Nesting of member functions, private member function, Arrays with in a class, Memory allocation for the objects, static data members, static member functions, Array of objects, objects as function argument, Friend function, returning an object. **Constructors and Destructors:** Constructors, Parameterized constructors, multiple constructors in a class, Constructors with default arguments, Dynamic initialization of objects, copy constructor, destructors. TEXT 1	11	L1,L2,L3.
3	**Operator overloading:** Overloading of unary operators and overloading of Binary operators, overloading binary operators using friends**.** **Inheritance:** Introduction, Defining derived classes, single inheritance, Making private function inheritable, multilevel inheritance, multiple inheritance, Hierarchical inheritance, Hybrid inheritance, virtual base class, abstract class. TEXT 1	11	L1,L2,L3,L4

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
4	**Exception Handling:** Introduction, basics of exception handling, Exception handling mechanisms, throwing mechanisms, catching mechanisms, Rethrowing an exception, specifying Exceptions, Exceptions in constructors and destructors. **Pointers, virtual functions and polymorphisms:** Introduction, pointers, pointers to objects, this pointer, pointers to derived classes, virtual functions, pure virtual functions, virtual constructors and destructors. TEXT 1	10	L1,L2,L3
5	**Working with files:** Introduction, classes for file stream operations, opening and closing a file, detecting a file, file pointer and their operations, sequential input and output operations, updating a file: Random access, Error handling during file operations and command line arguments. TEXT 1	10	L1,L2,L3

Note 1: Unit 2 and Unit 3 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 To gain the knowledge of object oriented concepts and get familiarized with basic concepts of programming.

CO2 Ability to design the programs using the classes and managing the objects.

CO3 Ability to design the programs with features of extensibility and reusability.

CO4 Ability to develop the programs with built in error handling capabilities.

CO5 Performing file operations.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO6

CO2 PO6

CO3 PO6

CO4 PO6, PO12

CO5 PO6, PO12

Text Books.

1 E. Balaguruswamy ,"Object oriented programming with C++", Fifth Edition, Tata McGraw Hill, 2012

Reference Text Books.

1 Stanley B.Lippmann, JoseeLajore, "C++ Primer", 4th Edition, Addison Wesley, 2005

2 Paul J Deitel, Harvey M Deitel, "C++ for Programmers", edition, Pearson Education, 2009

3 Herbert Schildt, "The Complete Reference C++", 4th Edition, Tata McGraw Hill, 2003

Web Links.

1. https://python.swaroopch.com/oop.html
2. https://www.codeproject.com › Development Lifecycle › Design and Architecture.
3. https://www.tcyonline.com/tests/object-oriented-programming/all/2

Subject Title : DSP Lab

Sub.Code: ECL57 No. of Credits:1.5=0:0:1.5 (L - T – P) No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs CIE+Assignment +SEE=50+0+50=100 Total No.of Contact Hours:39

Course Learning Objectives:

1 To analyze the sampling process, impulse response, convolution, frequency domain response of LTI systems
2 To analyze and design digital IIR and FIR filters
3 To demonstrate the DSP algorithms using Matlab software
4 To demonstrate the DSP algorithms using Code Composer Studio
5 Enter the course learning objective

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	1. Verification of sampling theorem. 2. Impulse response of a given system 3. Linear convolution of two given sequences. 4. Circular convolution of two given sequences 5. Autocorrelation of a given sequence and verification of its properties. 6. Cross correlation of given sequences and verification of its properties. 7. Solving a given difference equation. 8. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum. 9. Linear convolution of two sequences using DFT and IDFT. 10. Circular convolution of two given sequences using DFT and IDFT 11. Design and implementation of FIR filter to meet given specifications. 12. Design and implementation of IIR filter to meet given specifications. . TEXT 1 and TEXT 1	10	L1,L2,L3.
2	1. Linear convolution of two given sequences. 2. Circular convolution of two given sequences. 3. Computation of N- Point DFT of a given sequence 4. Noise: Add noise above 3 KHz and then remove; Interference suppression using 400 Hz tone. 5. Impulse response of first order system. TEXT 2	11	L3,L4,L5

Note 1: Unit 3 and Unit 4 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Define and verify the sampling theorem, impulse response, convolution and frequency response of the system

CO2 Understand DFT, IDFT, Auto correlation and Cross correlation

CO3 Analyze and design digital IIR and FIR filters.

CO4 Demonstration of DSP algorithms using Matlab software.

CO5 Demonstration of DSP algorithms using Code Composer Studio software.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO3,PO4,PO5, PO11, PO12

CO2 PO1,PO2,PO3,PO4,PO5, PO11, PO12

CO3 PO1,PO2,PO3,PO4,PO5, PO11, PO12

CO4 PO1,PO2,PO3,PO4,PO5, PO11, PO12

CO5 PO1,PO2,PO3,PO4,PO5, PO11, PO12

Text Books.

1 Sanjeet K. Mitra, "Digital Signal Processing using MATLAB", Edition, TMH, 2001

2 B. Venkataramani and Bhaskar, "Digital Signal Processors", edition, TMH, 2002

Reference Text Books.

1 J. G. Proakis & Ingale, "Digital Signal Processing using MATLAB", edition, Mc Graw Hill, 2000

Subject Title : Analog Communication Lab

Sub.Code: ECL58 No. of Credits:04=0:0:1.5 (L - T – P) No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs CIE+Assignment +SEE=50+50=100 Total No.of Contact Hours:36

Course Learning Objectives:

1 To analyze the filter concepts in communication systems
2 To analyze and compare different analog modulation schemes.
3 To demonstrate the concepts of modulation and demodulations of AM
4 To demonstrate the concepts of modulation and demodulations of FM, PWM and PPM
5 To demonstrate the concepts of modulation and demodulations of PWM and PPM

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	Second order Butterworth LPF and HPF.	3	L1,L2
2	Second Order Butterworth BPF	3	
3	Second order Butterworth BEF.	3	
4	Design and test R-2R DAC using op-amp	3	
5	Design and test the Astable multivibrator for given frequency and duty cycle using IC 555.	3	
6	Amplitude modulation & Detection.	3	
7	Frequency modulation using 8038/2206. FM detection using PLL	3	
8	Pre-emphasis and De-emphasis.	3	
9	Pulse Amplitude Modulation & Demodulation	3	
10	Pulse Width modulation and Demodulation	3	
11	Pulse Position modulation and Demodulation	3	
12	Time division multiplexing of analog signals.	3	

Note 1: Text Book: 1 & 2

Course Outcomes:

CO1 Define the LPF,HPF and BPF
CO2 Analyze and design filters.
CO3 Demonstration of Modulation and Demodulation
CO4 Illustrate the analog Signals.
CO5 Design the R-2R DAC.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO3,PO4,PO5
CO2 PO1,PO2,PO3,PO4,PO5
CO3 PO1,PO2,PO3,PO4,PO5

CO4 PO1,PO2,PO3,PO4,PO5

CO5 PO1,PO2,PO3,PO4,PO5

Text Books.

1 Simon Haykins, "**An Introduction to Analog and Digital Communication**", First Edition, John Wiley, 2003

2 David A. Bell, "**Operational Amplifiers and Linear IC's**", Third Edition, Oxford Publisher, 2011

Subject Title : Analog and Mixed Mode VLSI Design

Sub.Code: EC61 No. of Credits:03=03:0:0 (L - T – P) No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:39

Course Learning Objectives:

1 Understand the concept of Analog Design and Data Converter Fundamentals.
2 Design and Mismatch Error Analysis of DAC Architectures.
3 Design and Mismatch Error Analysis of ADC Architectures.
4 Analysis of Current sources and sinks in VLSI perspective.
5 Analysis of Single stage amplifiers in VLSI perspective.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Introduction to Analog Design:** Why Analog, Why Integrated, Why CMOS, General Concepts: Levels of Abstraction, Robust Analog Design. Basic MOS Device Physics: General considerations, MOS I/V Characteristics, Second Order Effects, MOS Device Models. **Data Converter Fundamentals:** Analog versus Digital discrete time signals, Converting Analog signals to Digital signals, Sample and Hold Characteristics, DAC specifications, ADC specifications, Mixed signal layout issues. TEXT 1 TEXT 2	09	L1,L2,L3.
2	**Data Converter Architectures:** DAC architecture, Digital input code, Resistors string, R-2R ladder networks, Current steering, Charge scaling DACs, Cyclic DAC, Pipeline DAC. TEXT 2	07	L1,L2,L3.
3	**ADC Architecture:** Flash, 2-step flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC. TEXT 2	07	L2,L3,L4
4	Current Sources and Sinks: The current mirror, The Cascade Connection, Sensitivity Analysis, Transient response, other current sources & sinks. TEXT 1 TEXT 2	07	L2,L3,L4
5	**Single stage amplifiers:** Common source stage, Common Source stage with resistive load, Common Source stage with Diode connected load, Common Source Stage with Current Source load, Common Source stage with Triode load. TEXT 1	09	L2,L3,L4

Note 1: Unit 1 and Unit 5 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Understanding of Fundaments in Analog and Digital design

CO2 Analysis of DAC Architectures and Mismatch errors.

CO3 Ability of Analyse the ADC architectures and Mismatch Error

CO4 Ability to Analyse and Design of Current sources and sinks.

CO5 Ability to Analyse and Design of Single Stage Amplifiers.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO3, PO4

CO2 PO4, PO5

CO3 PO5, PO7

CO4 PO10, PO12

CO5 PO3, PO12

Text Books.

1 Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Twenty Fifth Reprint, TATA McGraw Hill, 2013.

2 R Jacob Baker, "CMOS Circuit Design, Layout and Simulation", PHI, 2005.

Reference Text Books.

1 Philip E Allen and Douglas R Holberg, "CMOS Analog Circuit Design", Second edition, Oxford University Press, 2004.

2 Adel Sedra and K C Smith, "Microelectronics Circuits", Fifth edition, Oxford University Press, 2009.

Web Links.

1 http://www.nptelvideos.in

Subject Title: **Digital Communication**		
Subject Code: **EC62**	No. of Credits**:4=4 : 0 : 0 (L-T-P)**	No. of lecture hours/week : **4**
Exam Duration: **3 hours**	CIE +Assignment + SEE = **45 + 5 + 50 =100**	Total No. of Contact Hours :**52**

Course objectives:

1. A brief overview of the digital communication system and the techniques of formatting the source signal.
2. Demonstrate key concepts like geometrical analysis of signals, probability of error, various receiver types in detection.
3. Understand and analyze different waveform coding techniques and applications and spread spectrum modulation.
4. Understand information on discrete PAM signals, ISI and adaptive equalization for data transmission.
5. Analyze and design of digital modulation techniques and performance analysis based on probability of error.

UNIT No	**Syllabus Content**	No of Hours	Blooms Taxonomy Level
1	**Introduction**: Sources and signals, Basic signal processing operations in digital communications, Channels for digital communication. **Detection and Estimation:** Model of Digital communication system, Gram-Schmidt Orthogonalization Procedure, geometric interpretation of signals, response of bank of correlators to noisy input, Detection of known signals in noise, probability of error, correlation receiver, matched filter receiver. **Text 1, Text 2 and Text 3**	**13**	**L1,L2,L3**
2	**Sampling Process:** Sampling Theorem, signal space interpretation, Quadrature sampling of Band pass signal, PAM, TDM. **Waveform Coding Techniques:** Pulse Code Modulation, channel noise and error probability, Quantization noise and Signal to Noise Ratio, robust quantization, DPCM, DM. **Text 1 & Text 2**	**12**	**L3,L4,L5**
3	**Base-Band Shaping for Data Transmission:** Discrete PAM signals, power spectra of discrete PAM signals, Inter Symbol Interference, Nyquist's criterion for distortion less base-band binary transmission, correlative coding, eye pattern. **Text 1 &Text 2**	**09**	**L3,L4,L6**
4	**Digital Modulation Techniques:** Digital Modulation formats. **Coherent binary modulation techniques:** Binary ASK, PSK, and FSK. Coherent Quadrature modulation techniques**:** Quadriphase-shift keying (QPSK). **Non-coherent binary modulation techniques:** Differential	**09**	**L2,L3,L4,L5**

	phase shift keying (DPSK). **Text 1 &Text 2**		
5	**Spread Spectrum Modulation:** Pseudo noise sequences, notion of spread spectrum, Principle of Direct Sequence Spread Spectrum (DSSS), frequency hop spread spectrum. **Multiplexing and Multiple Access:** FDMA, TDMA, CDMA and SDMA **Text 1 & Text 3**	**09**	**L2,L3,L4**

Note 1: Unit 1 and Unit 2 will have internal choice.

Note 2: Two assignments are evaluated for 5 marks: Assignment – 1 from Units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1. Able to understand System approach to Digital communication right at the foundation level.
CO2. Gain the knowledge on the signal space concepts, probability of error, and detection of signals.
CO3. Gain the knowledge on the waveform coding techniques and spread spectrum modulation.
CO4. Capable of analyzing Discrete PAM signals and its power spectra and knowledge on ISI and correlative coding.
CO5. Gain the knowledge on the Optimization between the bandwidth efficiency and power efficiency of a communication system.

COs	**Mapping with POs**
CO1	PO1,PO2,PO4,PO6
CO2	PO1,PO2, PO6
CO3	PO1,PO2,PO4,PO6
CO4	PO1,PO2PO3,PO4,PO5,PO6
CO5	PO1,PO2PO3,PO4,PO5,PO6

TEXT BOOKS:

1. Simon Haykins, "**Digital Communications**", 4th Edition, John Wiley, ***2008***(reprint).
2. Dr. K. N. Hari Bhat & Dr. D. Ganesh Rao, "**Digital communications**", 2nd Edition, Sanguine technical publications, ***2008***. (Reprint).
3. Bernard Sklar," **Digital communications**", 3rd Edition, Pearson education, ***2007***

REFERENCE BOOKS/WEBLINKS:

1. K.Sam Shanmugam, "**Digital and analog communication systems**",4th Edition, John Wiley, ***1996***.
2. John Proakis, Masoud Salehi," **Digital communications**", 5th Edition, Mac Graw Hill, ***2008***.
3. Barry, John R., Lee, Edward A., Messerschmitt, David G," **Digital communications**", 3rd Edition, Springer, ***2004***
4. B. P. Lathi, Zhi Ding, "**Modern Digital and Analog Communication Systems**", 4th Edition, Oxford, 2009.

Subject Title : Embedded Systems

Sub.Code: EC63 No. of Credits:03=03:0:0 (L - T – P) No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:39

Course Learning Objectives:

1 Understand the basic concepts of Embedded Systems.
2 Explain the need for embedded systems.
3 Explain the Characteristics and quality attributes of Embedded Systems.
4 Get exposure to an advanced microcontroller and Operating system concepts.
5 Analyse Embedded system industrial applications.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Typical Embedded System:** Definition, Embedded systems vs. General Computing Systems, Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components. TEXT 1 Click here to enter text.	08	L1,L2,L3.
2	**Characteristics and Quality Attributes of Embedded Systems:** Characteristics of an Embedded system, Quality attributes of Embedded Systems. **Hardware Software Co-Design and Program Modelling**: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, UML-Use case diagrams. TEXT 1	07	L1,L2,L3.
3	**ARM-32 bit Microcontroller family:** ARM Cortex-M3 Processor-Introduction, Overview of the Cortex-M3, Instruction Sets, LPC 1768 programming. TEXT 2	10	L1,L2,L3.
4	**Real-Time Kernels and Operating Systems:** Introduction, Tasks and Things, Programs and Processes, The CPU is a Resource, Threads, Sharing Resources, Foreground/Background Systems, The Operating System, The Real-Time Operating Systems (RTOS), Operating System Architecture. TEXT 3	08	L1,L2,L3.
5	**Case Study of Embedded Systems**: Digital camera, Embedded Systems in Automobile, Smart Card Reader, Automated Meter Reading System. TEXT 1	06	L1,L2,L3.

Note 1: Unit 1 and Unit 3 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Describe the structure of a Typical Embedded System.

CO2 Justify different characteristics, quality attributes and modelling Techniques of Embedded System design.

CO3 Understand how an advanced microcontroller is programmed.

CO4 Understand the concept of Real time kernels & operating system.

CO5 Evaluate the concept of industrial applications through case studies.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO3

CO2 PO1,PO2,PO3,PO4,PO5

CO3 PO1,PO2,PO3,PO4

CO4 PO1,PO2,PO3,PO4,PO5,PO12

CO5 PO1,PO2,PO3,PO4,PO5,PO6,PO7,PO12

Text Books.

1 Shibu K V, "Introduction to Embedded Systems", First Edition, Tata McGraw Hill Education Private Limited, 2009

2 Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", Second Edition, Newnes, (Elsevier), 2008

3 James K Peckol, "Embedded Systems – A contemporary Design Tool", edition, John Weily, 2008

Reference Text Books.

1 Raj Kamal, "Embedded Systems – Architecture, Programming and Design", edition, Mc Graw Hill, 2012

Web Links.

1 http://nptel.ac.in/

Subject Title : INFORMATION THEORY AND CODING

Sub.Code: EC64 No. of Credits:03=03:0:0 (L - T – P) No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:39

Course Learning Objectives:

1 To impart the basic concepts of information theory.
2 To be able to understand the concepts of source coding.
3 To be able to understand fundamental limits on performance of a communication system.
4 To be able to understand the need for error control coding.
5 To be able to understand the need for cyclic codes and other error control codes to reduce error.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**INFORMATION THEORY:** Introduction, Measure of information, Average information content of symbols in long independent sequences, Average information content of symbols in long dependent sequences. Markoff statistical model for information source, Entropy and information rate of mark-off source. TEXT 1 and TEXT 1	08	L1,L2,L3
2	**SOURCE CODING:** Encoding of the source output, Shannon's encoding algorithm, Source coding theorem, Huffman coding. (Only binary codes) TEXT 1	06	L1,L2
3	**FUNDAMENTAL LIMITS ON PERFORMANCE:** Communication Channels: Discrete communication channels, Continuous communication channels. Discrete memory less Channels, Mutual information, Channel Capacity, Channel coding theorem, Channel capacity Theorem. TEXT 1	08	L2,L3,L4,L5
4	**INTRODUCTION TO ERROR CONTROL CODING:** Introduction, Types of errors, examples, Types of codes, Linear Block Codes: Matrix description, Error detection and correction, Standard arrays and table look up for decoding. TEXT 1 and TEXT 1	09	L2,L3,L4
5	**Binary Cycle Codes**, Algebraic structures of cyclic codes, Encoding using an (n-k) bit shift register, Syndrome calculation. BCH codes, RS codes, Golay codes, Turbo codes, LDPC codes. TEXT 1	08	L2,L3,L4

Note 1: Unit 1 and Unit 4 will have internal choice

Note Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.

2: Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 To impart the basic concepts information theory, source coding, channel coding, error control coding and binary cyclic codes.

CO2 Able to apply information theory to source coding, channel coding and error control coding.

CO3 Able to analyze source coding efficiency, channel capacity, controlling of error and special coding techniques.

CO4 Able to evaluate source coding, channel coding, types of errors and also the special coding techniques.

CO5 Able to create new techniques for source coding and channel coding.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO3,PO6,PO12

CO2 PO1,PO2,PO3,PO4,PO6,PO12

CO3 P01, PO2,PO4,PO5,PO6,PO11, P12

CO4 PO1,PO2,PO3,PO4,PO6,PO12,PO13

CO5 PO1,PO2,PO3,PO4,PO6,PO12,PO13

Text Books.

1 K. Sam Shanmugam, "Digital and Analog communication systems ", Second Edition, John Wiley India Pvt, 1996

2 Simon Haykins, "Digital communication", Second edition, John Wiley India Pvt. Ltd, 2008

Reference Text Books.

1 Glover and Grant, "Digital Communications", 2nd , Pearson Ed, 2008

2 P.S Satyanarayana, "Information Theory and Coding", edition, Dyanaram Publications, Reprint 2001

3 Giridhar, "Information Theory and Coding", 2nd edition, Pooja Publications, 2006

4 Ranjan Bose, "Information Theory and coding and Cryptography", 2nd edition, TMH, 2009

Web Links.

1 http://nptel.ac.in/courses/117101053/ /

Sub Title : ARTIFICIAL NEURAL NETWORK		
Sub Code:EC651	**No. of Credits:4=4 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : 3 Hours	**CIE +Assignment + SEE = 45 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. To become familiar with the concepts of Neural Networks.
2. To understand the Analysis of different techniques in neural networks.
3. To study the concepts of the concepts of Prediction Networks.
4. To understand the concepts of Polynomial networks in Artificial Neural Networks.
5. To analyze the Optimization of different techniques.

UNIT No	Syllabus Content	No of Hours
1	Introduction, Fundamental concepts and Models of Artificial Neural systems, Biological Neural Networks, structure and function of single neuron, neural net architectures, neural learning, use of neural networks, Application of MATLAB in Neural Network.	12
2	Simple neural nets for Pattern Classification, Supervised learning Single Layer Feedback Networks, examples, Perceptron learning perceptions, linear separability, perceptions training algorithm Training algorithm: Hebb rule & Delta rule, guarantees of success, modifications.	11
3	Multiclass networks-I, multilevel discrimination, preliminaries, back propagation, setting parameter values, theoretical results.	09
4	Prediction networks, radial basis functions, polynomial networks, regularization, unsupervised learning, winner take all networks.	10
5	Optimization using hop filed networks, simulated annealing, random search, evolutionary computation.	10

Note 1: Unit 3 and Unit 4 will have internal choice.

Note 2:Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2. Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1. Understand the basic concepts of Neural Networks.
CO2. Analysis and development of different techniques in neural networks.
CO3. Analysis the concepts of Prediction Networks.
CO4. Understand and analysis of the concepts of Polynomial networks in Artificial
CO5. Neural Networks.
CO6. Design optimization of different techniques.

Cos	Mapping with POs
CO1	P01,P02,P05,PO6
CO2	P02,P07
CO3	P08,P09
CO4	P09,P10
CO5	P07,P09

TEXT BOOKS:

1. Kishan Mehrotra, C. K. Mohan, Sanjay Ranka,Penram, **"Elements of Artificial Neural Networks"**, ***1997.***
2. J. Zurada, Jaico, **"Introduction to Artificial Neural Systems"**, ***2003.***

REFERENCE BOOKS/WEBLINKS:

1. Simon Hayking, **"Neural Networks: A Comprehensive Foundation",**2nd Edition, PHI.
2. Laurene Fausett, **"Fundamentals of Neural Networks: Architecture, Algorithms and Applications",** Person Education, 2004.

Subject Title : Adaptive Signal Processing

Sub.Code: EC652 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 To understand the basic concept of adaptive filter and adaptive system
2 To be able to identify the geometrical significance of Eigenvectors and values
3 To analyse the Simple, Newton's and Steepest Descent Gradient search method to search performance surface
4 To study estimation of gradient component using Newton's, Steepest-descent methods and LMS algorithm
5 To be familiar with design of adaptive communication system, adaptive noise canceller and adaptive modeling in FIR digital filter synthesis

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**ADAPTIVE FILTERS:** The Filtering Problem, Linear Optimum Filters, Adaptive Filters, Linear filter structures, Approaches to the development of linear adaptive filters. **ADAPTIVE SYSTEMS:** Definition and characteristics, Areas of application, General properties, Open-and closed-loop adaptation, Applications of closed-loop adaptation, Example of an adaptive system. TEXT 1 and TEXT 2	10	L1,L2,L3.
2	**THE ADAPTIVE LINEAR COMBINER:** General description, Input signal and weight vectors, Desired response and error, the performance function, gradient and minimum mean-square error, Example of a performance surface, Alternative expression of the gradient, Decorrelation of error and input components. **PROPERTIES OF THE QUADRATIC PERFORMANCE SURFACE:** Normal of the input correlation matrix, Eigen values and Eigen vectors of the input correlation matrix, an example with two weights, geometrical significance of eigenvectors and Eigen values. TEXT 1 and TEXT 3	11	L2,L3,L4,L5
3	**SEARCHING THE PERFORMANCE SURFACE:** Methods of searching the performance surface, Basic ideal of gradient search methods, a simple gradient search algorithm and its solution, Stability and rate of convergence, The learning curve, and Gradient search by Newton's method in multidimensional space, Gradient search by the method of steepest descent, Comparison of learning curves. TEXT 1 and TEXT 3	12	L3,L4,L5
4	**GRADIENT ESTIMATION AND ITS EFFECTS ON ADAPTATION:** Gradient component estimation by derivate	10	L3,L4,L5

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	measurement, the performance penalty, Derivative measurement and performance penalties with multiple weights, variance of the gradient estimate, effects on the weight-over solution, excess mean-square error and time constants, mis-adjustment, comparative performance of Newton's and steepest-descent methods, Total mis-adjustment and other practical considerations. **THE LMS ALGORITHM:** Derivation of the LMS algorithm, convergence of the weight vector, an example of convergence, learning curve, noise in the weight-vector solution, mis-adjustment, performance. TEXT 1 and TEXT 3		
5	**ADAPTIVE MODELING AND SYSTEM IDENTIFICATION:** General description, Adaptive modeling of multipath communication channel, adaptive modeling in geophysical exploration, Adaptive modeling in FIR digital filter synthesis. **ADAPTIVE INTERFERANCE CANCELING:** The concept of adaptive noise canceling, stationary noise-canceling solutions, effects of signal components in the reference input, The adaptive interference canceller as a notch filter, The adaptive interface canceller as a high-pass filter. TEXT 1	11	L3,L5,L6

Note 1: Unit 4 and Unit 5 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Understand the basic concept of adaptive filter and adaptive system

CO2 Understand the design of adaptive linear combiner and Identify the geometrical significance of Eigenvectors and values.

CO3 Analyze the Simple, Newton's and Steepest descent Gradient search method to search performance surface.

CO4 Estimate the gradient component using Newton's, Steepest-descent methods and LMS algorithm.

CO5 Design of adaptive communication system, adaptive noise canceller and adaptive modeling in FIR digital filter synthesis.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO3,PO4

CO2 PO1,PO2,PO3,PO4

CO3 PO3,PO4,PO7,PO10

CO4 PO3,PO4,PO5,PO7,PO10

CO5 PO5,PO6,PO7,PO10,PO12

Text Books.

1 Bernard Widrow and Samuel D. Stearns, "Adaptive Signal Processing", Edition, Pearson Education, Asia, 2009

2 Simon Haykin, "Adaptive filter Theory", 4th edition, Pearson Education Asia, 2008

3 Alexander, Thomas S, "Adaptive Signal Processing: Theory and Applications", edition, Springer-Verlag New York, Inc. New York, NY, USA, 1986

Reference Text Books.

1 T. Adali and Simon Haykin, "Adaptive Signal Processing: Next Generation Solutions", edition, Wiley India, 2012

2 Johnn R. Treichler C. Richard Johnson, Jr. and Michael G. Larimore, "Theory and Design of Adaptive Filters", edition, PHI, 2002

Web Links.

1 http://www.nptelvideos.in/2012/12/adaptive-signal-processing.html

2 http://www.cs.tut.fi/~tabus/course/ASP/Lectures_ASP.html

3 http://www.signal.uu.se/Courses/CourseDirs/AdaptSignTF/Adapt04.html

Subject Title : DIGITAL SWITCHING SYSTEM

Sub.Code: EC653 No. of Credits:04=04:01:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 Analyze basic switching techniques used in telephone system.
2 Analyze the different types of calls in DSS
3 Analyze time division and space division switching techniques and integrate both to improve Performance the course learning objective
4 Analyze different signalling techniques associated with telephone network.
5 Analyze switching networks with various techniques.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**DEVELOPMENTS OF TELECOMMUNICATIONS**: Network structure, Network services, terminology, Regulation, Standards, telecommunications transmission, Power levels, Four wire circuits, Digital transmission, FDM, TDM . **EVOLUTION OF SWITCHING SYSTEMS:** Message switching, Circuit switching, Functions of switching systems, distributed frames, crossbar systems Electronic switching ,Digital switching system. ITEXT 1 and TEXT 2	11	L1,L2,L3.
2	**TELECOMMUNICATION TRAFFIC:** Unit of traffic, Congestion, Traffic measurement, Mathematical model, lost call systems, Queuing systems. **SWITCHING SYSTEMS FUNDAMENTALS** : Introduction Purpose of analysis, Basic central office linkages, Outside plant versus inside plant, Switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems DSS fundamentals Building blocks of a digital switching system, Basic call processing TEXT 1 and TEXT 2	11	L1,L2,L3.
3	**COMMUNICATION AND CONTROL:** Introduction scope Switching communication and control Basic functions of interface controller Basic functions of network control processor Basic functions of central processor call processing control architectures Centralized control Hierarchical control quasi distributed control. **SWITCHING SYSTEM SOFTWARE**: Introduction, Scope, Basic software architecture, Call models, Software linkages during call, Call features. TEXT 2 and TEXT 2	10	L1,L2,L3.
4	A Generic Digital Switching System Model: Introduction, Scope,	10	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	Hardware and Software architecture, Simple call through a digital system, Common characteristics of digital switching systems Analysis Report. TEXT 2		
5	Maintenance of Digital Switching System: : Introduction, Scope, Software maintenance, Interface of a typical digital switching system central office, System outage and its impact on digital switching system reliability, Impact of software patches on digital switching system maintainability, methodology for reporting and correction of field problems Upgrade process success rate, Number of patches applied per year, Diagnostic resolution rate, Reported critical and major faults corrected, A strategy improving software quality. TEXT 2	10	L1,L2,L3.

Note 1: Unit 1 and Unit 2. will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Ability to describe the basic fundamentals of a telecom system.

CO2 Ability to understand traffic management and resource design

CO3 Ability to describe the common switching techniques used in the telecommunications industry.

CO4 Ability to describe the maintenance of digital switching systems.

CO5 Ability to analyze the various types of connection links used by industry for telecommunication system worldwide.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2

CO2 PO2,PO3,PO4

CO3 PO2,PO3,PO4,PO6,PO7

CO4 PO4,PO6,PO7

CO5 PO3,PO4,PO6,PO7

Text Books.

1 JE FLOOd, "Telecommunication Systems",", First Edition, Pearson Education, 2002

2 Syed R Ali, "**Digital Switching Systems**, edition, publisher, 2002

Reference Text Books.

1 John C Bellamy , "**Digital Telephony**", 3rd , Wiley India, 2000

Web Links.

1 http://nptel.ac.in/ online course /digital switching systems

2 https://books.google.co.in/books/about/Digital_Switching_Systems K Chandrashekar"Digital Switching Systems

3 https://www.youtube.com/watch?v=oOMlwW4rBz8/jeflood

Subject Title : POWER ELECTRONICS

Sub.Code: **EC654** No. of Credits: **4=4:0:0:0(L-T-P)** No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 To get an overview of different types of power semi-conductor devices and their switching characteristics.

2 To understand the operation, characteristics and performance parameters of controlled Rectifiers.

3 Understand the fundamental principles of basic power electronic converters.

4 To describe the need and functions of different types of power electronics converters.

5 Learn the basic concepts of operation of dc-dc converters, AC voltage controllers.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	POWER SEMICONDUCTOR DEVICES: Introduction, Applications of power electronics, Power semiconductor devices, Control characteristics, Types of power electronics circuits, Peripheral effects. characteristics of SCR,TRIAC,IGBT,MOSFET. TEXT 2	10	L1,L2,L3.
2	**INTRODUCTION TO THYRISTORS:** Principle of operation states, anode cathode characteristics, Two transistor model. Turn-on Methods, Dynamic Turn-on and turn-off characteristics, Gate characteristics. TEXT 2	11	L1,L2,L3.
3	**THYRISTOR TURN OFF METHODS**: Natural commutation, Forced commutation, Self commutation, Class A and Class B commutation, Complementary commutation, Auxiliary commutation, External pulse commutation, AC line commutation, Numerical problems. TEXT 2	12	L1,L2,L3.
4	**CONTROLLED RECTIFIERS:** Introduction, Principles of phase controlled converter operation, 1 φ semi converters with R-load, 1φ fully controlled converters with R-load, Numerical Problems. **AC VOLTAGE CONTROLLERS:** Introduction, Principles of on and off control, Principles of phase control, Single phase controllers with restive loads, numerical problems. TEXT 2 and TEXT 3	10	L1,L2,L3.
5	**DC CHOPPERS:** Introduction, Chopper classification, Principles of step down and step up choppers, , Numerical problems. **INVERTERS:** Introduction, Principles of Half Bridge Inverter with R and RL load, Performance parameters, Single Phase Bridge	11	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	Inverter with Resistive load. TEXT 1,2,3		

Note 1: Unit 3 and Unit 4 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Identify and Define the different types of Power Electronics devices

CO2 Explain the construction, working and characteristics of various power electronics Devices.

CO3 Determine and evaluate current, power, voltage of power electronic circuit such as converters and inverters

CO4 Analyse different power converter and inverter circuits and to Illustrate the application of Power Electronics devices .

CO5 Design Power converter and inverter circuits and assess the suitable switch choices for a given applications.

Course Outcomes Mapping with Programme Outcomes.

CO1 Po1

CO2 PO1

CO3 PO2, PO6, PO3

CO4 PO10, PO12

CO5 PO10, PO12

Text Books.

1 Ned Mohan, Tore M. Undeland, William P Robbins, "Power Electronics: Converters, Applications, and Design", John Wiley and Sons Inc.,, New York, ***2003***.,

2 Rashid M.H., "**Power Electronics Circuits, Devices and Applications** ", Prentice Hall , India, New Delhi, 2004.

3 Joseph Vithayathil, e, "**Power Electronics, Principles and Applications**", Tata McGraw-Hill Edition, 2010.

Reference Text Books.

1 Daniel W Hart,"Power Electronics", Tata McGraw Hill, New Delhi, 2010.

2 Joseph Vithayathil, "Power Electronics", New Age International (P) Limited, New Delhi, 2010.

3 Singh M.D., Khanchandani K B, **"Power Electronics**", Tata McGraw Hill, 2nd Edition, New Delhi, ***2007***.

4 Dr.P.S.Bimbra., "**Power Electronics**", Khanna Publications, 3rd Edition, ***2003.***

Sub Title : Advanced Communication Lab		
Sub Code: ECL66	**No. of Credits:1.5 =0:1.5 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE + SEE = 50 + 50 =100**	**Total No. of Contact Hours :36**

Course objectives:

1. Design and conduct an experiment on ASK,FSK,PSK, in communication systems.
2. Design and conduct an experiment on DPSK.
3. Design and conduct an experiment on QPSK
4. Establish Analog and Digital communication link using optical fiber
5. Understand the concepts of modulation and demodulations like Yagi Antenna, Directional coupler

UNIT No	Syllabus Contents	No of Hours
1.	ASK generation and detection using discrete components.	3
2.	FSK generation and detection using discrete components.	3
3.	PSK generation and detection using discrete components.	3
4.	To prove sampling theorem, To study the effects of under sampling and oversampling.	3
5.	DPSK generation and detection using kit.	3
6.	QPSK generation and detection using kit	3
7.	Establish Analog and Digital communication link using optical fiber and Measure the losses (coupling loss, bending loss, attenuation loss numerical aperture.)	3
8.	Measurement of frequency, guide wavelength, power, VSWR and Attenuation in a microwave test bench.	3
9.	Measurement of directivity and gain of micro strip patch antenna using printed dipole.	3
10.	Measurement of directivity and gain of Yagi antenna (printed) using printed dipole.	3
11.	Determination of coupling and isolation characteristics of a micro strip directional Coupler.	3
12.	Measurement of resonance characteristics of a micro strip ring resonator and determination of dielectric constant of the substrate.	3

Course Outcomes:

CO1. Understanding the concept of Antenna

CO2. Understanding the generation and manipulation of signals using analog modulation schemes

CO3. Able to understand the concepts of modulation and demodulations like ASK

CO4. Able to understand the concepts of modulation and demodulations like FSK

CO5. Able to understand the concepts of modulation and demodulations like QPSK.

Cos	Mapping with POs
CO1	PO1,P02,PO3
CO2	PO1,PO4,PO5
CO3	PO4,P12,PO8
CO4	PO9,P010,P011
CO5	PO3,PO6,PO7,PO10

REFERENCE BOOKS/WEBLINKS:

1. George Kennedy, " Electronic Communication Systems", TMH 4th Edition, 2008.

Subject Title : Embedded System Lab

Sub.Code: ECL67 No. of Credits:1.5=0:1.5:0 (L - T – P) No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs CIE +SEE=50+50=100 Total No.of Contact Hours:36

Course Learning Objectives:

1 To study the features of LPC 1768 MCU.
2 Develop the Assembly level programming of ARM Cortex M3 Processor.
3 Develop the Embedded C level programming of ARM Cortex M3 Processor.
4 Understand Interfacing of different modules to LPC 1768 MCU.
5 Develop 32-bit microcontroller based Embedded system applications.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	Write a Assembly language program to link Multiple object files and link them together.	3	L1, L2
2	The Assembly language program i. To calculate the value of the function. ii. To store data in desired Memory location.	3	L1,L2,L3.
3	Write a C program to Output the message using UART.	3	L1, L2, L3,L4
4	Write a C Program to interface LED using LPC 1768.	3	L1, L2, L3, L4
5	Write a C Program to interface Relay using LPC 1768.	3	L1, L2, L3, L4
6	Write a C Program for DC motor/Stepper motor rotation using LPC 1768.	3	L1, L2, L3, L4
7.	Write a C program to interface a Real Time Clock (RTC) of LPC 1768.	3	L1, L2, L3, L4
8.	Write a program to read on-chip ADC value and display it on UART terminal using LPC 1768.	3	L1, L2, L3, L4
9	Write a C program to interface a DAC of LPC 1768.	3	L1, L2, L3, L4
10	Generation of PWM signal for motor control using LPC 1768.	3	L1, L2, L3, L4
11	Write a C program to Design a Stopwatch using interrupts.	3	L1, L2, L3, L4
12	Write a C program to interface Keypad using LPC 1768.	3	L1, L2, L3, L4

Course Outcomes:

CO1 Understanding features of the architecture of ARM Cortex M3.
CO2 Create assembly, Embedded C level programs of ARM Cortex M3.
CO3 Interface different modules to LPC 1768 MCU.
CO4 Design and testing a program for Different Embedded applications.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2, PO6

CO2 PO2, PO3, PO4, PO5, PO12

CO3 PO2, PO3, PO4, PO12

CO4 PO2, PO3, PO4, PO5,PO12

References Text Books.

1 Joseph Yiu, "**The Definitive Guide to the ARM CORTEX-M3**", Second Edition, Newnes , **2008**

2 NXP Semiconductors, "**LPC17xx user manual**", Choose an item.

3 Micro-CM3768, "**ARM Cortex-M3 Development Board User Manual**

Note: Programming to be done using Keiluvision 4 and download the program on to a M3 evaluation board such as NXP LPC1768.

Sub Title : MINI PROJECT WORK		
Sub Code:ECP68	**No. of Credits:02=0 :0 :02 (L-T-P)**	
Exam Duration :03 Hour	**CIE + SEE = 50+50 =100**	**Total No. of Contact Hours : 03**

A student is required to carry out elaborated project work. The project may be either design and fabrication work or a simulation of a problem on a computer. At the end of the semester student will be required to submit a detailed report of literature survey, design problem formulation, work plan and work done and will defend his/her work carried out before the examiners at the time of final evaluation.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(EFFECTIVE FROM ACADEMIC YEAR 2017-18)
Scheme of Teaching for VII Semester B.E(E & C) (2014 Batch)

Subject Code	Title	Teaching Dept.	Contact hours/week				Examination		
			Theory	Tutorial	Practical	No of credits	CIE	SEE	Total Marks
EC71	Optical Fiber Communication	EC	03	00	00	03	50	50	100
EC72	Computer Communication Network	EC	04	00	00	04	50	50	100
EC73X	Elective-2 (Group B)	EC	04	00	00	04	50	50	100
EC74X	Elective-3 (Group C)	EC	04	00	00	04	50	50	100
ECEXX	Institute Elective-1 (Group-1)	EC	04	00	00	04	50	50	100
ECL75	VLSI Lab	EC	00	00	03	1.5	50	50	100
ECL76	CCN Lab	EC	00	00	03	1.5	50	50	100
ECP77	Project Phase-1	EC	00	00	01	-	-	-	-
		TOTAL	**20**	**00**	**07**	**22**	**350**	**350**	**700**

DEPARTMENTAL ELECTIVE SUBJECTS

SUBJECT CODE	ELECTIVE -2 (Group B) Credits- 4
EC731	Nano Electronics
EC732	Wireless Sensor Network
EC733	DSP Algorithms & Architecture
EC734	Image Processing
EC735	Wireless Communication

SUBJECT CODE	ELECTIVE -3 (Group C) Credits- 4
EC741	Multimedia Communication
EC742	Speech Processing
EC743	Operating System
EC744	Operation Research
EC745	Robotics

INSTITUTE ELECTIVE SUBJECTS

SUBJECT CODE	ELECTIVE -2 (Group B) Credits- 4
ECE01	Cryptography
ECE02	Automotive Safety measurements
ECE06	Mechatronics
ECE07	Robotics And Machine Vision System

CHAIRMAN (BOS) **DEAN (ACADEMIC)** **PRINCIPAL**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(EFFECTIVE FROM ACADEMIC YEAR 2016-17) **Scheme of Teaching for VIII Semester B.E (E & C) (2014 Batch)**

Subject Code	Title	Teaching Dept.	contact hours/week				Maximum Marks		
			Theory	Tutorial	Practical	No of credits	CIE	SEE	Total Marks
HS04	Intellectual Property Rights	MBA	02	00	00	02	50	50	100
EC81x	Elective-4 (Group D)	EC	04	00	00	04	50	50	100
EC8XX	Institute Elective-2 (Group- II)	EC	04	00	00	04	50	50	100
ECS82	Seminar	EC	00	00	02	02	50	-	050
ECP83	Project Work	EC	00	00	00	12	100	100	200
		TOTAL	**10**	**00**	**00**	**24**	**300**	**250**	**550**

DEPARTMENTAL ELECTIVE SUBJECTS	
SUBJECT CODE	**ELECTIVE -2 (Group B) Credits- 4**
EC811	Satellite Communication
EC812	Cryptography and Network Security
EC813	Real Time Operating System
EC814	Adhoc Wireless Networks
EC815	Datastructure using C++
EC816	Virtual Instrumentation

INSTITUTE ELECTIVE SUBJECTS	
SUBJECT CODE	**Subject Title(Group-2) Credits- 4**
ECE03	Semiconductor Fabrication
ECE04	Wireless sensor Network
ECE05	Mobile communication
ECE08	Sensors

CHAIRMAN (BOS) **DEAN (ACADEMIC)** **PRINCIPAL**

Subject Title : Optical fiber communication

Sub.Code: EC71 No. of Credits:03=03:0:0 (L - T – P) No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:43

Course Learning Objectives:

1 To become familiar with the basic concepts of propagation of optical energy in single and multimode optical fibers.
2 To understand the fiber losses and its measurements to provide background for optical fiber communications.
3 To study the concepts of the optical fiber fabrication techniques and cable design.
4 To understand the the optical sources and detectors.
5 To become familiar with the optical Networks and its communication.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**OVERVIEW OF OPTICAL FIBER COMMUNICATION:** Introduction, Historical development, general system, advantages, disadvantages, and applications of optical fiber communication, optical fiber waveguides, Ray theory transmission: total internal reflection, acceptance angle, numerical aperture ,skew rays, Cylindrical fiber: modes, mode coupling, step index fibers and graded index fibers, single mode fibers: cutoff wave length and mode filed diameter. TEXT 1 Click here to enter text.	07	L1,L2,L3.
2	**TRANSMISSION CHARACTERISTICS OF OPTICAL FIBERS:** Introduction, **A**ttenuation, Material absorption: Intrinsic and extrinsic absorption, linear scattering losses: Rayleigh scattering and Mie scattering, Dispersion: Chromatic dispersion: Material and Waveguide dispersion, bending loss. . TEXT 1	07	L1,L2,L3.
3	**OPTICAL FIBERS AND CABLES:** Cable design: Fiber buffering, cable structural and strength members, cable sheath and water barrier, examples of fiber cables. **OPTICAL SOURCES AND DETECTORS: Laser** :Introduction, basic concepts: absorption and emission of radiation, population inversion. Optical emission from semiconductors: The p-n junction, spontaneous emission, carrier recombination, stimulated emission and lasing, heterojunctions, semiconductor materials. **LED:** Introduction, power & efficiency: double heterojuncation LED **Detectors:** Introduction, quantum efficiency, responsivity. Semiconductor photodiodes: p-i-n and Avalanche photodiode, Phototransistors, photoconductive detectors. responsivity. Semiconductor photodiodes: p-i-n and Avalanche photodiode, Phototransistors, photoconductive detectors. TEXT 1	09	L1,L2,L3,L4
4	**DIGITAL TRANSMISSION SYSTEMS:** Point –to-point links: System considerations, Link power Budget, Rise Time Budget, First window transmission distance, Transmission distance for single mode	07	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	Links TEXT 2		
5	**OPTICAL NETWORKS:** Introduction, Optical networks concepts: Optical networking terminology, Optical network node and switching elements, Optical network transmission modes, layers and protocols: Synchronous networks, Asynchronous transfer mode, internet protocol, Optical network deployment: Long haul networks, Metropolitan area networks, Access networks, Local area networks. Optical Ethernet, Network protection, restoration and survivability. TEXT 1	09	L1,L2,L3,L4

Note 1: Unit 3 and Unit 5 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Describe the basic concepts of propagation of optical energy in single and multimode optical fibers.

CO2 Compare the fiber losses and its measurements to provide background for optical fiber communications.

CO3 Use the optical fiber fabrication techniques and cable design

CO4 Identify the optical sources and detectors.

CO5 Understanding and Identifying the different optical Networks and its communication.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2,PO6,PO10,PO11,PO12

CO2 PO2,PO6,PO10,PO11,PO12

CO3 PO2,PO6,PO10,PO11,PO12

CO4 PO2,PO6,PO10,PO11,PO12

CO5 PO2,PO6,PO10,PO11,PO12

Text Books.

1 John M. Senior, "**Optical Fiber Communications**", 3rd Impression Reprint v, Pearson Education, 2012

2 Gerd Keiser, "**Optical Fiber Communication**", 3rd Ed.,, MGH, Reprint, 2012

Reference Text Books.

1 Joseph C Palais, "**Fiber Optic Communication**", 4th Edition, Pearson Education, 2012

2 GowerJohn , "Optical Communication System", second edition, Prentice, *2013*

Web Links.

1 www.google.com, Optical Fiber Communications", John M. Senior pdf
2 www.google.com, optical fiber communication gerd keiser 4th edition pdf
3 www.nptelcoursematerial
4 Nptel.ac.in/lectures/courses/117101002
5 www.youtube/opticalfibercommunication

Subject Title : Computer Communication Networks(CCN)

Sub.Code: EC72 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 To understand working of networks, mechanics of TCP/IP architecture
2 To elaborates the background concepts, and functionalities of application layer, transport layer, and network layer.
3 To study and analyse the flow and error control schemes.
4 To present ample details about the protocols, technologies, algorithms and standards that are used by each layer as it relates to the internet.
5 To overview LAN concept, link layer , connecting LANs and connecting devices.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	Computer Networks and the Internet: What Is the Internet? The Network Edge, The Network Core, Delay, Loss, and Throughput in Packet-Switched Networks, Protocol Layers and Their Service Models, Networks Under Attack, History of Computer Networking and the Internet TEXT 1 Click here to enter text.	10	L1,L2,L3.
2	**Application Layer:** Principles of Network Applications, The Web and HTTP, File Transfer: FTP, Electronic Mail in the Internet, DNS—The Internet's Directory Service, Peer-to-Peer Applications, Socket Programming: Creating Network Applications TEXT 1	10	L1,L2,L3.
3	**Transport Layer:** Introduction and Transport-Layer Services, Multiplexing and Demultiplexing, Connectionless Transport: UDP, Principles of Reliable Data Transfer, Connection-Oriented Transport: TCP, Principles of Congestion Control, TCP Congestion Control. TEXT 1	12	L1,L2,L3.
4	**The Network Layer:** Introduction, Virtual Circuit and Datagram Networks, What's Inside a Router? The Internet Protocol (IP): Forwarding and Addressing in the Internet, Routing Algorithms, Routing in the Internet, Broadcast and Multicast Routing TEXT 1	10	L1,L2,L3
5	**The Link Layer: Links, Access Networks, and LANs:** Introduction to the Link Layer, Error-Detection and -Correction Techniques, Multiple Access Links and Protocols, Switched Local Area Networks, Link Virtualization: A Network as a Link Layer, Data Center Networking, Retrospective: A Day in the Life of a Web Page Request. **Wireless and Mobile Networks:** Introduction, Wireless Links and Network Characteristics, WiFi: 802.11 Wireless LANs, Cellular Internet Access, Mobility Management: Principles, Mobile IP,	10	L1,L2,L3

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	Managing Mobility in Cellular Networks, Wireless and Mobility: Impact on Higher-Layer Protocols TEXT 2		

Note 1: Unit 2 and Unit 3 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Identify the layered tasks, wireless and mobile networks for data transmission.

CO2 Explain the functionalities of application layer, transport layer , network layer, Wireless and Mobile Networks

CO3 Summarize the Wireless and Mobile Networks

CO4 Analyze the functions of network layer and design of addressing schemes.

CO5 Characterize the various functions of transport layer and application layer.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2, PO4, PO7,PO11,PO12

CO2 PO2, PO4, PO7,PO11,PO12

CO3 PO2, PO4, PO7,PO11,PO12

CO4 PO2, PO4, PO7,PO11,PO12

CO5 PO2, PO4, PO7,PO11,PO12

Text Books.

1 James F. Kurose, Keith W. Ross, "**Computer Networks**", Pearson Education, 2nd Edition, **2003**.

2 B. Forouzan , " **Data Communication and Networking**", TMH, 4th Edition, ***2006***.

Reference Text Books.

1 Russel Bradford, "**The Art of Computer Networking"**, Pearson Education, Ist Edition, **2007**.

Web Links.

1 nptel.ac.in/courses/106105081/1

2 http://www.bau.edu.jo/UserPortal/UserProfile/PostsAttach/10617_1870_1.pdf

Sub Title : Nano-Electronics		
Sub Code: EC731	**No. of Credits:4=4 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : 3 Hours	**CIE +Assignment + SEE = 45 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. To learn and understand basic and advance concepts of nanoelectronics.
2. To introduce the students to nanoelectronics, nanodevices, spintronics and molecular electronics. To be able to understand the Photolithography and Etching
3. To identify quantum mechanics behind nanoelectronics.
4. To describe the principle and the operation of nanoelectronic devices.
5. To explain the principle and application of nano devices.

UNIT No	Syllabus Contents	No of Hours
1	**Basics of nanoelectronics** – capabilities of nanoelectronics – physical fundamentals of nanoelectronics – basics of information theory – the tools for micro and nano fabrication – basics of lithographic techniques for Nanoelectronics. **Text1**	10
2	**Quantum electron devices –** from classical to quantum physics: upcoming electronic devices – electrons in mesoscopic structure – short channel MOS transistor – split gate transistor – electron wave transistor – electron spin transistor – quantum cellular automate – quantum dot array – Principles of Single Electron Transistor (SET) – SET circuit design – comparison between FET and SET circuit design. **Text1**	10
3	**Nanoelectronics with tunneling devices and superconducting devices –** tunneling element technology - RTD: circuit design based RTD – Defect tolerant circuits. Molecular electronics – elementary circuits – flux quantum devices – application of superconducting devices – Nanotubes based sensors, fluid flow , gas temperature; Strain –oxide nanowire, gas sensing (ZnO,TiO2,SnO2,WO3), LPG sensor (SnO2 powder)- Nano designs and Nanocontacts – metallic nanostructures. **Text1**	11
4	A survey about the limits – Replacement Technologies – Energy and Heat dissipation – Parameter spread as Limiting Effect – Limits due to thermal particle motion – Reliability as limiting factor – Physical limits – Final objectives of integrated chip and systems. **Text1**	10
5	**Memory devices and sensors –** Nano ferroelectrics – Ferroelectric random access memory – Fe-RAM circuit design – ferroelectric thin film properties and integration – calorimetric sensors – electrochemical cells – surface and bulk acoustic devices – gas sensitive FETs – resistive semiconductor gas sensors – electronic noses – identification of hazardous solvents and gases – semiconductor sensor array.**Text1**	11

Note 1. Unit 3 and Unit 5 will have internal choice.

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2 Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1. Identify the fundamental science and quantum mechanics behind nano-electronics
CO2. Ability to Interpret the concepts of a quantum well, quantum transport and tunnelling effects.
CO3. Creation of microelectronics and nanoelectronics.
CO4. Ability to comparison between FET and SET circuit design
CO5. Create the Nanoelectronics with tunneling devices and superconducting devices

CO6: Ability to Conclude the applications of nanotechnology and nanoelectronics.

Cos	**Mapping with POs**
CO1	PO5,PO7,PO8
CO2	PO7,PO8,PO10
CO3	PO5,PO8,PO12
CO4	PO5,PO9,PO11
CO5	PO9,PO11,PO12
CO6	PO5,PO9,PO11, PO12

TEXT BOOK:

1. Karl Goser, Peter Glosekotter, Jan Dienstuhl., **"Nanoelectronics and Nanosystems",** Springer, 2004
2. Mick Wilson, Kamali Kannangara, Geoff Smith, Michelle Simmons, Burkhard Raguse **"Nanotechnology: basic science and emerging technologies"**, Overseas Press (2005)

REFERENCE BOOKS/WEBLINKS:

1. Rainer Waser (ed.) **"Nanoelectronics and information technology : Advanced electronic materials and novel devices (2nd edition)" ,** Wiley VCH Verlag Weiheim (2005)
2. Rainer Waser, **"Nanoelectronics and Information Technology (edition, 2005)",** John Wiley & Sons, Germany.
3. K. Goser, **"Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices"** (Edition, 2004), Springer. London

Subject Title : Wireless Sensor Network

Sub.Code: EC732 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 Students will be able to describe the unique issues in sensor networks.
2 Students will be able to describe current technology trends for the implementation and deployment of wireless sensor networks.
3 Students will be able to discuss the challenges in designing MAC, routing and transport protocols for wireless sensor networks.
4 Interpret the goals for different protocols
5 Students will be able to describe and implement protocols

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	Introduction: Unique Constraints and Challenges, Advantages of Sensor Networks, Energy advantage, Detection advantage, Sensor Network Applications, Habitat monitoring, Wildlife conservation through autonomous, non-intrusive sensing, Tracking chemical plumes, Ad hoc, just-in-time deployment mitigating disasters, Smart transportation: networked sensors making roads safer and less congested, Collaborative Processing.. TEXT1	10	L1, L2,L4
2	**Canonical Problem: Localization and Tracking,** A Tracking Scenario, *Sensing Model, Collaborative Localization, Bayesian State Estimation,* Distributed Representation and Inference of States: *Impact of Choice of Representation, Design consideration in Distributed Tracking,* Tracking Multiple Objects: *State-Space Decomposition, Data Association,* Sensor Models, Performance Comparison and Metrics , TEXT 1	10	L1, L2,L4,L5
3	Networking Sensors: Key Assumptions, Medium Access Control, General Issues, Geographic, Energy-Aware Routing: Unicast Geographic Routing, Routing on a Curve, Energy-Minimizing Broadcast, Energy-Aware Routing to a Region, Attribute-Based Routing. **Infrastructure Establishment:** Topology Control, Clustering, Time Synchronization, Localization and Localization Services, **Sensor Tasking and Control :**Task-Driven Sensing ,Roles of Sensor Nodes and Utilities Information-Based Sensor Tasking Sensor Selection IDSQ: Information-Driven Sensor Querying ,Cluster Leader–Based Protocol ,Sensor Tasking in Tracking Relations TEXT 1	13	L1,L2,L3,L4,L5
4	Sensor Network Databases: Sensor Network Databases,	10	L1,L4,L5

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	Sensor Database Challenges, Querying The Physical Environment, Query Interfaces, Cougar sensor database and abstract data types, Probabilistic queries, High-level Database Organization, In- Network Aggregation, Query propagation and aggregation, Tiny DB query processing, Query processing scheduling and optimization, Data-Centric Storage, Data Indices and Range Queries, One-dimensional indices, Multidimensional indices for orthogonal range searching, Non-orthogonal range searching, Distributed Hierarchical aggregation, Multi-resolution, Partitioning, Fractional cascading, Locality preserving hashing, Temporal Data, Data aging, Indexing motion data. TEXT 1		
5	Sensor Network Platforms: Sensor Node Hardware, Sensor Network Programming Challenges, Node-Level Software Platforms, Node-Level Simulators, Programming Beyond Individual Nodes: State-Centric Programming, and Tools Applications and Future Directions: Emerging Applications, Future Research Directions TEXT 1	08	L1,L2,L6

Note 1: Unit 1 and Unit 3 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Define WSN, identify issues related to different protocols for WSN

CO2 Understand protocols require for Wireless Sensor Network

CO3 Explore current sensor technologies through algorithms, protocols, and applications

CO4 Analyse routing ,tracking problems, data base requirement and programing challenges

CO5 Interpret the design goals consideration tracking and evaluate the performance of different protocols for wireless Sensor Network Click here to enter text.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO5,PO6,PO10

CO2 P01, PO2, PO5,PO8

CO3 P01, PO4,PO5,PO6

CO4 P01, PO2,PO3

CO5 PO2, PO5,PO6,PO9

Text Books.

1 Feng Zhao, Leonidas Guibas, "Wireless Sensor Networks, An Information Processing Approach", Elsevier, 2004

Reference Text Books.

1 Kazem Sohrabi,Daniel Minoli.Taieb Znati "Wireless Sensor Networks", Wiley Inter science, Wiley India, 2007

Web Links.

1 https://onlinecourses.nptel.ac.in/noc17_cs07

Subject Title : DSP Algorithms and Architecture

Sub.Code: EC733 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 To gain the knowledge of basics of DSP like FIR filters, IIR filters, FFT algorithms, architectures of DSP processors and interfacing to other devices
2 To interpret the basics of DSP like FIR filters, IIR filters, FFT algorithms, architectures of DSP processors and interfacing to other devices
3 To apply the concept of FIR filters, IIR filters, FFT algorithms, architectures of DSP processors and interfacing to other devices
4 To illustrate the basics of DSP like FIR filters, IIR filters, FFT algorithms, architectures of DSP processors and interfacing to other devices
5 To design and implement the FIR filters, IIR filters, FFT algorithms on DSP processor.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Introduction to Digital Signal Processing:** Introduction, a Digital Signal-Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. **Architectures for Programmable Digital Signal Processors:** Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing. TEXT 1	12	L1, L2
2	**Programmable Digital Signal Processors:** Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54xx., Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and Programming, On-Chip peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor. TEXT 1	10	L1,L2
3	**Implementation of Basic DSP Algorithms:** Introduction, The Q-notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). TEXT 1	10	L2,L3,L4
4	**Implementation of FFT Algorithms:** Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit-Reversed Index Generation & Implementation on the TMS32OC54xx. **Interfacing Memory and Parallel I/O Peripherals to DSP Devices:** Introduction, Memory Space Organization, External Bus	11	L2,L3,L4

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I / O Direct Memory Access (DMA). TEXT 1		
5	**Interfacing and Applications of DSP Processor:** Introduction, Synchronous Serial Interface, A CODEC Interface Circuit. DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System. TEXT 1	09	L3,L4,L5

Note 1: Unit 1 and Unit 4 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Define the fundamentals of DSP and the general architecture of DSP

CO2 Understand the general architecture of DSP processor and in particular TMS320C54xx DSP to run algorithms.

CO3 Applying the concept of DSP algorithms when they are run on processors.

CO4 Analyze the implementation of FFT algorithms and interfacing memory to DSP processor.

CO5 Creating new designs based on existing algorithms targeted to DSP processor.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2, PO3, PO4, PO5,PO11,PO12

CO2 PO2, PO3, PO4, PO5,PO11,PO12

CO3 PO2, PO3, PO4, PO5,PO11,PO12

CO4 PO2, PO3, PO4, PO5,PO11,PO12

CO5 PO2, PO3, PO4, PO5,PO11,PO12

Text Books.

1 Avatar Singh and S. Srinivasan, "Digital Signal Processing", Third Edition, Thomsoc Learning, 2004

Reference Text Books.

1 Ifeachor E. C., Jervis B. W Pearson-Education, "Digital Signal Processing: A Practical Approach", edition, Pearson Education, 2002

2 B Venkataramani and M Bhaskar, "Digital Signal Processors", 2nd edition, TMH, 2010

3 Peter Pirsch, "Architectures for Digital Signal Processing", 4th edition, John Wiley, 2007

Web Links.

1 http://bwrcs.eecs.berkeley.edu/Classes/CS252/Notes/Lec09-DSP.pdf

2 http://nptel.ac.in/courses/117102060/

Subject Title : Image processing

Sub.Code: EC734 No. of Credits:04=4:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 Describe image representation in spatial domain.
2 Compare Different image transforms used in different domains of Image Processing.
3 Illustrate improvement of the quality of images by using different filtering techniques
4 Identify filtering techniques to restore image from degraded images.
5 Conversion of colour images from one model to another model and design different techniques of image compression

Prentice Hall of India, Eastern Economy Edition

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	DIGITAL IMAGE FUNDAMENTALS: Definition of Image processing. Some examples of fields that use Digital Image processing, Fundamental Steps in Digital Image Processing: Components of an Image processing system, Image sensing and acquisition, Image Sampling and Quantization, Basic Relationships between Pixels, Mathematical tools used in Digital Image Processing: Array Vs Matrix operation, Linear Vs Nonlinear Operations, Arithmetic operations, Set & Logical operations Text 1	8	L1,L2,L3.
2	**IMAGE TRANSFORMS:** Introduction, Two-dimensional orthogonal & unitary transforms, Properties of unitary transform, Two dimensional Discrete Fourier transform. The Cosine Transform, Sine transform, Hadamard transform, Haar transform. Text 2	10	L1,L2,L3.
3	**INTENSITY TRANSFORMATIONS & SPATIAL FILTERING:** Basics of Intensity transformation and spatial filtering, Basic Intensity transformation functions, Histogram processing, Enhancement using Arithmetic/Logic Operations, Fundamentals of Spatial filtering, Smoothing Spatial filters, Sharpening spatial filters. **FILTERING IN THE FREQUENCY DOMAIN**: Filtering in the frequency domain, Smoothing using Frequency Domain filters, Sharpening using Frequency Domain filters, Homomorphic filtering. Text 1	12	L1,L2,L3.
4	**IMAGE RESTORATION:** A Model of image degradation/restoration process, Noise models, Restoration in the Presence of Noise only-Spatial Filtering, Periodic Noise Reduction by Frequency Domain Filtering, Linear, Position-Invariant Degradations, Estimating the degradation functions,	10	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	Inverse filtering, Minimum mean square error (Weiner) Filtering. TEXT 1		
5	**COLOUR IMAGE PROCESSING**: Color fundamentals , Colour models: RGB Color model, CMY & CMYK Color models, The HSI Colour model, Pseudo colour Image Processing, Basics of full color Image Processing. **IMAGE COMPRESSION**: Fundamentals of coding redundancy, spatial and temporal redundancy, irrelevant information, measuring image information, fidelity criteria, image compression models, JPEG Encoder and decoder using DCT technique, image formats, containers and compression models, Some basic compression methods: Huffman coding, arithmetic coding LZW coding. TEXT 1	12	L1,L2,L3.

Note 1: Unit 3 and Unit5will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Identify image representation in spatial domain.

CO2 Summarise various image transforms applied in Image Processing

CO3 Apply different techniques to improve quality of images

CO4 Apply filtering techniques to restore images from degraded images

CO5 Modify color images from one model to another model and asses different techniques of image compression.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2, PO11, PO12

CO2 PO5,PO6,PO7, PO11, PO12

CO3 PO5,PO6,PO7, PO11, PO12

CO4 PO5,PO6,PO7, PO11, PO12

CO5 PO5,PO6,PO7, PO11, PO12

Text Books.

1 Rafael C Gonzalez,"Richard E Woods, Digital Image Processing", Third Edition, Prentice Hall India , 2008.

2 Anil K Jain,, "Fundamentals of Image Processing", Fourth Edition Prentice Hall India,2009.

Reference Text Books.

1 B. Chanda and D. DuttaMajumdar,, "Digital Image Processing and Analysis",, Prentice Hall of India, Eastern Economy Edition, 2004

2 S.Shridhar "Digital Image processing", Oxford university Press , 2011

3 S.Jayaraman, S. EsakkiRajan and T.Veerakumar, “Digital Image Processing”, Tata McGaw Hill , 2009.

Web Links.

1. nptel.ac.in/courses/117105079/
2. www. Eee.tufts.edu
3. www.clarifai.com
4. www.cis.rit.edu/class/simg361
5. www.pearsonhiheredu.com

Subject Title : Multimedia Communication

Sub.Code: EC741 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 Describe the ways in which multimedia information is captured, Processed, and rendered
2 Discuss the ways in which multimedia data is transmitted across networks
3 Introduce Multimedia Quality Of Service (QOS) and to compare subjective and objective methods of assessing user satisfaction
4 Discuss privacy and copyright issues in the context of multimedia
5 Understand audio and video compression standards

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Multimedia Communications:** Introduction, Multimedia Information Representation, Multimedia Networks, Multimedia Applications, Media Types, Communication Modes, Network Types, Multipoint Conferencing, Network QOS Application QOS.TEXT 1	12	L1
2	**Multimedia Information Representation:** Introduction, Digital Principles, Text, Images, Audio, Video. TEXT 1	10	L1
3	**Text And Image Compression:** Introduction, Compression Principles, Text Compression, Image Compression. TEXT 1	10	L1,L2
4	**Audio And Video Compression:** Introduction, Audio Compression, DPCM, ADPCM, APC, LPC, Video Compression, Video Compression Principles, H.261, MPEG, MPEG-1, And MPEG-2. TEXT 1	12	L1,L2
5	**Multimedia Information Networks:** Introduction, Lans, Ethernet, Token Ring, Bridges, FDDI High-Speed Lans, LAN Protocol. TEXT 1	08	L1

Note 1: Unit 1 and Unit 4 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Define Multimedia Representation, Types And Applications.

CO2 Understanding the digital principles, Image and Video features and its characteristics.

CO3 Understanding the image and text compression techniques as well as audio video standards.

CO4 Analyze the multimedia network and its parameters and characteristics.

CO5 Ability to understand Audio and Video Compression.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2, PO6

CO2 PO2, PO6, PO7

CO3 PO2, PO4, PO6, PO7, PO12

CO4 PO2, PO6

CO5 PO2, PO6,PO7

Text Books.

1 Fred Halsall, "**Multimedia Communications: Applications, Networks, Protocols And Standards**", Second Edition Reprint, Thomson Learning Pearson Education, Asia, 2002

Reference Text Books.

1 Nalin K. Sharda, "**Multimedia Information Networking**", Second Edition, PHI, 2003

2 Ralf Steinmetz, Klara Narstedt, "**Multimedia Fundamentals: Vol 1 - Media Coding And Content Processing**", First Edition, Pearson Education, 2004

Subject Title : Speech Processing

Sub.Code: EC742 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 To define the digital models of speech signals, time domain models of speech processing, Fourier transforms, linear predictive coding of speech and homo morphic speech processing.
2 To interpret the digital models of speech signals, time domain models of speech processing using Fourier transforms and to understand linear predictive coding of speech and homo morphic speech processing
3 To apply the Fourier transforms to speech signals and to predict using linear predictive coding of speech and homo morphic speech processing.
4 To illustrate digital models of speech signals, time domain models of speech processing, Fourier transforms, linear predictive coding of speech and homo- morphic speech processing.
5 To design linear predictive coding of speech and homo morphic speech processing.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	Digital models for speech signal: Introduction, The process of speech production, The Mechanism of speech production, Acoustic phonetics, Digital models for speech signalsDigital Representations of speech wave form: Sampling of speech signals, Instantaneous quantization, Adaptive quantization.TEXT1	10	L1, L2,L4
2	Time domain models for speech processing: Introduction, Time dependent processing of speech, short time energy and average magnitude , short time Average zero crossing rate, Speech vs. Silence discrimination using Energy and Zero crossings, Pitch period estimation using parallel processing approach,, short-time autocorrelation function.TEXT1	10	L1, L2,L4
3	**Short-time Fourier analysis :** Introduction, definitions and properties: Fourier Transforms interpretation and linear filter interpretation, sampling rates in time and frequency. Filter bank summation and overlap add methods for short time synthesis of speech, sinusoidal and harmonic plus noise method of analysis/synthesis.TEXT1	10	L1,L2,L3,L4,L5
4	**Linear predictive coding of speech:** Introduction, Basic principles of Linear Predictive analysis, Solution of the LPC Equations- Cholesky method-Dublin's Recursive solution, Applications of LPC parameters- Pitch detection using LPC parameters, Formant Analysis- LPC Vocoder-Voice excited voice Vocoder. TEXT1	11	L1,L2,L3,L4,L5
5	**Homo morphic speech processing**: Introduction, homomorphic system for convolution, the complex	11	L1,L2,L3,L6

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	cepstrum of speech, homo morphic vocoder **Digital speech processing for man – machine communication by voice:** Introduction, Voice response systems, speaker recognition system, speech recognition systems.		

Note 1: Unit1and Unit5will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Define the digital models of speech signals, time domain models of speech processing, Fourier transforms, linear predictive coding of speech and homo morphic speech processing.

CO2 Interpret the digital models of speech signals, time domain models of speech processing using Fourier transforms and to understand linear predictive coding of speech and homo morphic speech processing.

CO3 Apply the Fourier transforms to speech signals and to predict using linear predictive coding of speech and homo morphic speech processing..

CO4 Illustrate digital models of speech signals, time domain models of speech processing, Fourier transforms, linear predictive coding of speech and homo morphic speech processing.

CO5 Design linear predictive coding of speech and homo morphic speech processing , Evaluate the speech processing algorithms for applications.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO5

CO2 P01, PO2,PO5,

CO3 P01, PO4,PO5

CO4 P01, PO2

CO5 PO2,PO4,PO5,PO12

Text Books.

1 L. R. Rabiner and R.W. Schafer, “Digital Processing of Speech Signals”, Choose an item., Pearson Education Asia, 2004

Reference Text Books.

1 Dr.Shailad D. Apte, “Speech and Audio Processing”, 2012 REPRINT, Wiley India, 2012

2 T. F. Quatieri, “Discrete time speech signal processing ”, Pearson Education Asia, 2002

3 Gold and N. Morgan, “Speech and Audio signal Processing: Processing and Perception of Speech and Music”, John Wiley India Pvt. L, 2004

Web Links.

1 http://nptel.ac.in/syllabus/117104023/

Subject Title : Operating Systems

Sub.Code: ECxx No. of Credits:04=04:01:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 Understand the history and types of operating systems.
2 Understand the design issues associated with operating systems development.
3 Understand the process management and scheduling.
4 Understand the concepts of memory management.
5 Understand the file and I/O operation.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**INTRODUCTION :** Goals of an O.S, Operation of an O.S **OVERVIEW OF OPERATING SYSTEMS:**, OS and computer system, Efficiency, system performance and user convenience, Classes of operating systems, O.S and the computer system, Batch processing system, Multi programming systems, Time sharing systems, Real time operating systems. TEXT 1 Click here to enter text.	10	L1,L2
2	**STRUCTURE OF THE OPERATING SYSTEMS:** Operation of an O.S, Structure of an operating system, Operating systems with monolithic structure, Layered design of an operating system, Virtual machine operating systems, Kernel based operating systems. TEXT1	10	L1,L2
3	**PROCESS MANAGEMENT:** Process and programs, Programmer view of processes, OS view of processes, Threads. **SHEDULING:** Preliminaries, Non pre-emptive scheduling policies, pre-emptive scheduling policies, scheduling in practice. TEXT 1	11	L1,L2,L3.
4	**MEMORY MANAGEMENT:** Managing the memory hierarchy, static and dynamic memory allocations, memory allocation to a process, reuse of memory, contiguous and non contiguous memory allocation, paging, segmentation, segmentation with paging. **VIRTUAL MEMORY:** Virtual memory Basics, Demand paging, page replacement policies. TEXT 1	11	L1,L2,L3.
5	**FILE SYSTEMS:** File system and IOCS, Files and file organization, Fundamentals of file organizations, Directory structures, File protection, Interface between file system and IOCS, and Allocation of disk space. TEXT 1	10	L1,L2

Note 1: Unit 3 and Unit 4 will have internal choice
Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Ability to understand the evolution of operating systems and various types of operating systems in practice.

CO2 Ability to understand different styles operating system development.

CO3 Ability to understand the concepts of process and scheduling management.

CO4 Ability to understand the design issues in memory management.

CO5 Ability to understand the file and I/O management techniques.

Course Outcomes Mapping with Programme Outcomes.

CO1 Po7

CO2 Po10

CO3 Po12

CO4 Po12

CO5 Po12

Text Books.

1 D.M.Dhamdhare, "**Operating Systems**", Second Edition, TMH, 2008

Reference Text Books.

1 Stalling William, "Operating Systems", Sixth edition, Pearson Education, Choose an item.

2 Avi Silberchatz, Peter Baer Galvin, Greg Gagne, "Operating system Concepts", Ninth edition, John wiley & Sons

Web Links.

1 faculty.salina.k-state.edu/tim/ossg/Introduction/OSrole.html

2 https://users.dimi.uniud.it/~antonio.dangelo/OpSys/.../Operating_System_Concepts.pdf

Subject Title : Operation Research

Sub.Code: **EC744** No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 To be able to understand Scope of Operations Research and TP Formulation

2 To be able to understand the Assignment Problem.

3 To be able to understand the Network Construction

4 To be able to classify the type Game Theory

5 To be able to understand the Queuing system and their characteristics

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Introduction to Operations Research:** Basics definition, scope, objectives, phases, models and limitations of Operations Research. Transportation Problem: Formulation, solution, unbalanced Transportation problem. Finding basic feasible solutions – Northwest corner rule, least cost method and Vogel's approximation method. Optimality test: the stepping stone method and MODI method.**Text1**	11	L1,L2
2	**Assignment model:** Formulation. Hungarian method for optimal solution. Solving unbalanced problem. Traveling salesman problem and assignment problem. **Text1**	11	L1,L2
3	**PERT-CPM Techniques:** Network construction, determining critical path, floats, scheduling by network, project duration, variance under probabilistic models, prediction of date of completion, crashing of simple networks. **Text1**	10	L1,L2
4	**Game Theory:** Formulation of games, Two person-Zero sum game, games with and without saddle point, Graphical solution (2x n, m x 2 game), dominance property. **Text1**	10	L1,L2
5	**Queuing Theory:** Queuing system and their characteristics. The M/M/1 Queuing system, Steady state performance analyzing of M/M/ 1 and M/M/C queuing model. **Text1**	10	L2,L3

Note 1: Unit 1 and Unit 2 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Identify the OR Definitions and Able to apply TP.

CO2 Ability to interpret and explain the Assignment Problem.

CO3 Creation of Network construction, determining critical path, floats and scheduling by network

CO4 Ability to Compare the type of 2x n, m x 2 game.

CO5 Design the Queuing system, Game Theory and their characteristics.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO5,PO7,PO8

CO2 PO7,PO8,PO10

CO3 PO5,PO8,PO12

CO4 PO5,PO9,PO11

CO5 PO9,PO11,PO12

Text Books.

1 P. Sankara Iyer, "**Operations Research**", First Edition, Tata McGraw-Hill, ***2008***

2 A.M. Natarajan, P. Balasubramani, A. Tamilarasi, "**Operations Research**", First Edition, Pearson Education, ***2005***

Reference Text Books.

1 P. K. Gupta and D. S. Hira, "**Operations Research**", Second Edition, S. Chand & co, ***2007***

2 J K Sharma, "**Operations Research, Problems and Solutions**", Third Edition, Macmillan India Ltd, ***2010***

Subject Title : Robotics

Sub.Code: EC745 No. of Credits:04=4:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 Explanation of Architecture and Comparison of Microprocessors and Microcontrollers.
2 Architecture of microcontroller 8051, its features and memory organization.
3 Addressing modes and Programming of Microcontroller of 8051.
4 Peripherals of Microcontroller and real-time applications of Microcontroller 8051
5 Advanced Microprocessor and Microcontrollers, its features and applications.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Basic Configuration of Robotics and its Working** Introduction – definition – basic configuration of robotics and its working –robot components – manipulator, end effectors, drive system, controller, sensors –mechanical arm – degrees of freedom – links and joints – construction of links, types of joint – classification of robots – Cartesian, cylindrical, spherical, horizontal articulated (SCARA), vertical articulated – structural characteristics of robots –work envelope and work volume - robot work volumes and comparison – wrist rotations – mechanical transmission, pulleys, belts, gears, harmonic drive – conversion between linear and rotary motion and its devices. TEXT 1 and TEXT 2	08	L1, L2
2	**Robot Controller, Servo Systems** Robot controller – level of controller – open loop and closed loop controller –servo systems — robot path control – point to point – continuous path control – sensor based path control – controller programming – actuators – dc servo motors – stepper motors – hydraulic and pneumatic drives - feedback devices – potentiometers – optical encoders – dc tachometers	13	L1,L2,L3.
3	**Robot Motion Analysis and Vision System** Robot motion analysis – robot kinematics – robot dynamics - end effectors –grippers and tools - gripper design – mechanical gripper – vacuum gripper –magnetic grippers – sensors – transducers – tactile sensors – proximity sensors and range sensors – force and moment sensors and its applications and problems photoelectric sensors – vision system – image processing and analysis – robotic applications – robot operation aids – teach pendent – MDI and computer control	15	L1, L2, L3,L4
4	**Robot programming** Robot programming – lead through methods and textual robot languages – motion specification - motion interpolation - basic robot languages – generating of robot programming languages –	15	L1, L2, L3, L4

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	On-Line & Off-Line programming - robot language structure – basic commands – artificial intelligence and robotics.		
5	**Robot Application in Manufacturing** Robot application in manufacturing – material handling –assembly finishing –adopting robots to work station - requisite and non – requisite robot characteristics –stages in selecting robot for individual application – precaution for robot –future of robotics. Economics analysis for robotics – cost data required for the analysis – methods of economic analysis – pay back method – equivalent uniform annual cost method – return on investment method.	14	L1, L2

Note 1: Unit 3 and Unit 4 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Understanding various Microprocessor and microcontroller architecture and features.

CO2 Explaining the memory organization and addressing modes of Microprocessors and Microcontrollers.

CO3 Writing a program in Assembly level and high-level languages using instructions of Microcontroller for the real time applications.

CO4 Interfacing various peripherals to the microcontroller 8051.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2, PO4, PO5, PO11, PO12

CO2 PO2, PO4, PO5, PO11, PO12

CO3 PO4, PO5, PO11, PO12

CO4 PO4, PO5, PO11, PO12

Text Books.

1 Mikkel P.Groover, Mite chell weiss, Rogern Negal and Nicholes G.Odress, "Industrial Robotics Technology- Programming and Applications ", First Edition, Spectrum Publisher, 1997

2 R.K.Mittal, I.J.Nagrath , "Robotics and controls ", 2nd edition, Tata Mcgraw Hill Education Pvt. , 2005

3 Ali Mazidi, Janice Gillespie Mazidi and Rollin D. McKinlay , "The 8051 Microcontroller and Embedded Systems – using assembly and C"", edition, PHIChoose an item., 2006

4 Enter name, "Book title", edition, publisher, year

5 Enter name, "Book title", edition, publisher, 2014

Reference Text Books.

1 Doughlaes –R. HAlcoojr, "An Introduction to robotics", edition, publisher, year

2 "Book title", edition, publisher, year

Web Links.

Subject Title : VLSI LAB

Sub.Code: ECL75 No. of Credits:=0:0:1.5:0(L - T – P) No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs CIE+Assignment +SEE=50 Total No.of Contact Hours:39

Course Learning Objectives:

1 Able to understand the simulation and synthesis of digital circuits such as Basic gates, Universal gates, Flip Flops, Counters.
2 Able to design Analog Inverter circuit and verify.
3 Able to design different types of Analog Amplifiers and verify.
4 Able to design Operational Amplifier and verify.
5 Able to draw Layouts of Amplifiers.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	Write RTL Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library under the given Constraints. Do the initial timing verification with gate level simulation. i. An Inverter ii. A Buffer iii. Transmission Gate iv. Basic/universal gates v. Flip flop -SR, D, JK, MS and T. vi. 4-bit counter [Synchronous and Asynchronous counter] TEXT 1	12	L1,L2,L3
2	Design an Inverter with given specifications, completing the design flow mentioned below: a. Draw the schematic and verify the following i. DC Analysis ii. Transient Analysis b. Draw the Layout and verify the DRC and Check for LVS TEXT 1	06	L1,L2,L3, L4
3	Design the following circuits, completing the design flow mentioned below: i) A Single Stage differential amplifier ii) Common source amplifier iii)Common Drain amplifier a. Draw the schematic and verify the following. i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC and LVS	15	L1,L2,L3, L4

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	TEXT 2 & TEXT 3		
4	Design an op-amp using given differential , Common source and Common Drain amplifier in library and completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii). AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC and LVS. TEXT 2 & TEXT 3	06	L1,L2,L3, L4

Course Outcomes:

CO1 To impart the concepts of simulation and synthesis of digital circuits.

CO2 Will be able apply the concepts of simulation and synthesis of digital circuits and understand the Inverter in Analog Perspective.

CO3 Will be able to design and analyze Amplifiers in Analog Perspective.

CO4 Will be able evaluate different amplifiers.

CO5 Will be able create layout and verify Amplifiers.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2,PO3, PO4,PO5,PO7,PO12

CO2 PO2,PO3, PO4,PO5,PO7,PO12

CO3 PO2,PO3, PO4,PO5,PO7,PO12

CO4 PO2,PO3, PO4,PO5,PO7,PO12

CO5 PO2,PO3, PO4,PO5,PO7,PO12

Text Books.

1 Douglas A. Pucknell & Kamran Eshraghian , "Basic VLSI Design Principles and Practice", 3rd Edition, PHI, 2005

2 Neil H. E. Weste, K. Eshragian, "Principles of CMOS VLSI Design - A Systems Perspective.", 3rd Edition, Pearson Education (Asia) Pvt. Ltd, 2005

3 R. Jacob Baker, "CMOS Circuit Design, Layout and Simulation", 3rd edition, John Wiley India Pvt. Ltd, 2008

Sub Title: COMPUTER COMMUNICATION NETWORKS LABORATORY		
Sub Code:ECL76	**No of Credits : 0:0:1.5:0**	**No of lecture hours/week : 3**
Exam Duration :03Hours	**Exam Marks : 50**	**Total No of lecture hours: 13**

Course Learning Objectives(CLOs)

1.	To be able to perform experiment to simulate stuffing /de-stuffing, Encryption/ Decryption of message.
2.	To be able to perform experiment to simulate spanning tree and shortest path algorithm.
3.	To be able to perform experiment to simulate polynomial code checksum for CRC-CCITT.
4.	To be able to perform experiment to simulate various LAN protocols.
5.	To be able to perform experiment to simulate serial using data communication kit.

EX. NO.	**Syllabus**	**No of Hours**
1	Write a C program to implement Bit Stuffing and Character Stuffing.	3
2	Write a C program to implement Encryption and Decryption of Substitution and transposition cryptographic algorithms.	3
3	Write a C program to implement Cyclic Redundancy checksum.	3
4	Write a C program to implement Minimum Spanning Tree algorithm.	3
5	Write a C program to implement Shortest path Algorithm.	3
6	Study and analyze the performance of CSMA/CD protocol using NETSIM.	3
7	Study the performance of network with CSMA/CA protocol and compare with CSMA/CD protocol	3
8	Implement and analyze the Stop-and-wait protocol using LAN TRAINER KIT.	3
9	Compare and Contrast the performance of Go Back N and Selective protocols using LAN TRAINER KIT.	3
10	Cable a network according to the given network topology and test and verify configurations using packet tracer by using ping commands.	3
11	Configuring Wireless LAN Access and test and verify configurations using packet tracer.	3
12	Configuring Traditional Inter-VLAN Routing and test and verify configurations using packet tracer.	3
13	Serial communication using DCT.	3
	TOTAL HOURS	**39**

Programme Outcomes (POs)	
1	Able to perform experiment to simulate stuffing /de-stuffing bit frame and character frame data: coded using C/C++.
2	Able to perform experiment to simulate spanning tree and shortest path algorithm: coded using C/C++.
3	Able to perform experiment to simulate polynomial code checksum for CRC-CCITT: coded using C/C++.
4	Able to perform experiment to simulate Encryption and Decryption of message: coded using C/C++.
5	Able to perform experiment to simulate Serial and parallel communication using data communication kit.

Relationship to the Program Outcomes(POs)

Course Outcomes (COs)	**Program Outcomes (POs)**
CO1	PO5,PO6,PO7
CO2	PO5,PO6,PO7
CO3	PO5,PO6,PO7
CO4	PO5,PO6,PO7
CO5	PO5,PO6,PO7

Subject Title : SATELLITE COMMUNICATION

Sub.Code: EC811 No. of Credits: 4=4 : 0 : 0 (L-T-P) No. of Lecture Hours/Week : 4
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:56

Course Learning Objectives:

1 To be able to familiar with satellite systems and laws governing satellite orbit.
2 To understand concept of geostationary orbit and various losses on signal transmission in satellite system.
3 To evaluate link power budget estimation, System noise and various space segment subsystems.
4 To study earth segment, interference between satellite circuits and multiple access systems.
5 To understand Direct Broadcast System, Satellite mobile and specialized services.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**OVER VIEW OF SATELLITE SYSTEMS:** Introduction, frequency allocation, INTELSAT , Orbits and launching methods : Kepler's laws, definitions of terms for earth orbiting satellites. Orbital element, apogee and perigee heights, orbit perturbations, inclined orbits, calendars, universal time, sidereal time, orbital plane, local mean time and sun synchronous orbits. Numerical problems. **Text 1, Reference 1**	10	L1, L2
2	**GEOSTATIONARY ORBIT:** Introduction, antenna, look angles, polar mount antenna, Limits of visibility, earth eclipse of satellite, sun transit outage, launching orbits. Numerical problems. **Text 1 , Ref. 1** **RADIO WAVE PROPAGATION:** Atmospheric losses, ionospheric effects, rain attenuation. **Text 1**	10	L1,L2
3	**SPACE SEGMENT:** Introduction, power supply unit, attitude control: spinning satellite stabilization, momentum wheel stabilization. Station keeping, thermal control, TT&C subsystem, transponders, antenna subsystem. **SPACE LINK:** Introduction, EIRP, transmission losses: free space transmission, feeder losses, and antenna misalignment losses. Link power budget equation, System noise: antenna noise, amplifier noise temperature, overall system noise temperature. CNR, effects of rain. **Text 1, Ref. 2**	10	L1,L2,L3
4	**EARTH SEGEMENT:** Introduction, receive only home TV system: out-door unit, indoor unit, MATV, CATV, Tx – Rx earth station. Text 1 **INTERFERENCE AND SATELLITE ACCESS:** Introduction, interference between satellite circuits. S**atellite access**: single access, Pre-assigned FDMA, demand assigned FDMA, spade system, TDMA: pre-assigned TDMA, demand assigned TDMA, down link analysis, comparison of uplink	14	L2,,L3

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	power requirements for TDMA & FDMA. **Text 1**		
,l55	**DIRECT BROADCAST SATELLITE SERVICES:** Introduction, orbital spacing, power rating and number of transponders, frequency and polarization, transponder capacity, bit rates for digital TV, **SATELLITE SERVICES:** satellite mobile services, VSAT, RadarSat, Global positioning satellite system, orbcomm. **Text 1**	13	L1,L2,L3

Note 1 **Unit 3 and Unit 4 will have internal choice.**

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Identify the characteristics of satellite communication Orbits, Launching Methods and channels.

CO2 Explain the concept of geostationary orbit and mathematical model for various losses on signal transmission in satellite system.

CO3 Apply analytical and empirical models in the design of satellite networks and space segments. Able to compute link power budget estimation, System noise.

CO4 Illustrate the multiple access schemes for satellite access.

CO5 Compile the Direct Broadcast System, satellite mobile and specialized services

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1, PO2

CO2 PO1, PO2, PO6

CO3 PO2, PO6, PO12

CO4 PO2, PO6, PO12

CO5 PO2, PO6, PO12

Text Books.

1 Dennis Roddy, “Satellite Communications”,4th Edition, McGraw- Hill International edition, 2006,

Reference Text Books.

1 Timothy Pratt, Charles Bostian and Jeremy Allnutt, “Satellite Communications”, 2nd Edition, John Wiley Pvt. Ltd & Sons, 2008.Pearson Education Asia / PHI, Indian Reprint, 1997.

2 W. L. Pitchand, H. L. Suyderhoud, R. A. Nelson. , “‘Communication Systems””, 2nd Edition, Pearson Education , 2007

Web Links.

1 https://www.amazon.com/Satellite-Communications-2nd-Dennis-Roddy/.../00705337...

3 https://www.flipkart.com/satellite-communications-2nd/p/itme9z9vfzvc9gea

Subject Title : Cryptography and Network Security

Sub.Code: EC812 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 To impart the basic concepts of network security and classical encryption, number theory, stream ciphers, block ciphers and authentication.
2 To interpret the cryptographic algorithms like stream ciphers and block ciphers using classical encryption techniques
3 To apply the concept of classical encryption techniques to stream ciphers and block ciphers
4 To analyze the stream ciphers and block ciphers and their applications in network security
5 To design the stream ciphers and block ciphers for applications in network security

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Introduction:** Services, mechanisms and attacks, OSI security architecture, Model for network security. **Symmetric ciphers:** Symmetric Cipher Model, Substitution Techniques: Caesar Cipher, Mono Alphabetic Cipher, Playfair Cipher, Hill Cipher, polyalphabetic Cipher and One-Time Pad (OTP). Transposition Techniques, Rotor Machines, Steganography. TEXT 1	10	L1, L2
2	**Finite Fields:** Groups, Rings, Fields. Modular Arithmetic: Divisors, properties of modulo operator, modular arithmetic operations and properties. Euclid's Algorithm, Greatest Common Divisor (GCD), finding GCD. Finite Fields of the form GF (p): Finite fields of order p, finding multiplicative inverse in GF (p). Polynomial Arithmetic: Ordinary polynomial Arithmetic, polynomial Arithmetic with coefficients in Zp. Finding GCD. Finite fields of the form GF(2^n). TEXT 1	10	L1, L2
3	**Block Ciphers:** Simplified DES, Block Cipher Principles, Data encryption standard (DES), Strength of DES, Block Cipher Design Principles and Block Cipher Modes of Operation, Evaluation Criteria for Advanced Encryption Standard, The AES Cipher. TEXT 1	10	L2,L3,L4
4	**Block Ciphers:** Principles of Public-Key Cryptosystems, The RSA algorithm. Key Management, Diffie - Hellman Key Exchange. **Authentication functions and Hash Functions:** Authentication functions, message authentication codes, hash functions, security of Hash functions and MACs. TEXT 1	11	L2,L3,L4
5	**Web Security:** Web Security Consideration, Security socket layer (SSL) and Transport layer Security (TLS), Secure Electronic Transaction (SET).	11	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	Intruders: Intruders, Intrusion Detection, Password Management.. TEXT 1		

Note 1: Unit 1 and Unit 2 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Define the basic concepts of network security, classical encryption, number theory, Private key, public key, authentication and network security

CO2 Understand the structure of cryptographic algorithms and their applications.

CO3 Apply the concept of classical encryption techniques to existing standard algorithms.

CO4 Illustrate the significance of cryptographic algorithms and their applications in network security.

CO5 Design the private key and public key, authentication functions for applications in network security.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2,PO4,PO5,PO6,PO11, P12

CO2 P01, PO2,PO4,PO5,PO6,PO11, P12

CO3 P01, PO2,PO4,PO5,PO6,PO11, P12

CO4 P01, PO2,PO4,PO5,PO6,PO11, P12

CO5 P01, PO2,PO4,PO5,PO6,PO11, P12

Text Books.

1 William Stallings, "Cryptography and Network Security: Principles and Practice", Fifth Edition, Pearson Education, 2010

Reference Text Books.

1 Behrouz Forouzan, "Cryptography and Network Security", edition, TMH, 2007

2 Alfred J. Menezes, Paul C. Van Oorschot and Scott A. Vanstone, "Handbook of Applied Cryptography ", edition, CRC press, reprint 2001

3 Bruce Scheiner , "Applied cryptography: protocols, algorithms, and source code in C", 2nd edition, Wiley India, 2008

4 Atul Kahate, "Cryptography and Network Security", 2nd edition, TMH, 2006

Web Links.

1 http://www.nptel.ac.in/courses/106105031/

2 http://faculty.mu.edu.sa/public/uploads/1360993259.0858Cryptography%20and%20Network%20Security%20Principles%20and%20Practice,%205th%20Edition.pdf

Sub Title : Real Time Operating System		
Sub Code:EC813	**No. of Credits:4=4 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : O3Hhours	**CIE +Assignment + SEE = 45 + 05 + 50 =100**	**Total No. of Contact Hours : 52**

Course objectives:

1. To study the basic concepts of specialized processors
2. To study the various Scheduling strategies
3. To study multiresource services
4. To study the embedded system components
5. To understand design trade-offs

UNIT No	Syllabus Content	No of Hours
1	**Introduction to real-time embedded systems**: Brief history of real time systems, a brief history of embedded systems. **System Resources**: resource analysis, real-time service utility, scheduling classes, the cyclic executive, scheduler concepts, preemptive fixed priority scheduling policies, Real-Time OS, thread safe reentrant functions. Text1	10
2	**Processing**: preemptive fixed-priority policy, feasibility, rate montonic least upper bound, necessary and sufficient feasibility, deadline – monotonic policy, dynamic priority policies. **I/O Resources**: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture. Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems. Text1	12
3	**Multiresource Services**: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion. Soft Real-Time Services: Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services. Text1	08
4	**Embedded system components**: firmware components, RTOS system software mechanisms, software application components. Debugging components: exceptions assert, checking return codes, single-step debugging, kernel scheduler traces, test access ports, trace ports, power-on self test and diagnostics, external test equipment, application-level debugging. Text1	12
5	**High availability and reliability design**: reliability and availability, similarities and differences, reliability, reliable software, available software, design trade-offs, hierarchical applications for fail-safe design. Design of RTOS. Text1	10

Note 1: Unit 2 and Unit 4 will have internal choice.

Note 2: Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2. Assignment - 2 from units 3 and 4.

Course Outcomes:

CO1:List the basic concepts of specialized processors
CO2:Explain the various Scheduling strategies
CO3:Show the multiresource services
CO4: Illustrate the embedded system components.
CO5: Categorize the design trade-offs

Cos	Mapping with POs

CO1	PO1, PO2
CO2	PO2, PO6
CO3	PO2,PO6, PO10,P12
CO4	PO2,PO6, PO10,P12
CO5	PO2,PO6, PO10,P12

Text Books:

1. Sam Siewert, "**Real-Time Embedded Systems and Components**," Cengage Learning India Edition, ***2007***.
2. MykePredko, **" Programming and Customizing the PIC microcontroller" , 3rd Ed, TMH, *2000*.**
3. C. M. Krishna, Kang. G. Shin**,. "Real Time Systems", Mc Graw Hill, India, *1997***

REFERENCE BOOKS / WEBLINKS:

1. Raj Kamal, "**Embedded Systems**", Tata McGraw Hill, New Delhi, ***2008***.
2. Phillip. A. Laplante, "**Real-Time Systems Design and Analysis**", Prentice Hall India,2nd Edition, ***2005***.
3. Jane. W. S. Liu, "**Real Time Systems**", Pearson Education, ***2005***

Subject Title : ADHOC Wireless Network

Sub.Code: EC814 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 To define Adhoc network, identify issues in protocol for Ad hoc wireless Networks
2 To understand different protocols for Ad hoc wireless Networks To demonstrate scheduling mechanism and flooding mechanism.
3 To analyse MAC protocol, routing protocol, transport protocol Ad hoc wireless Networks
4 Interpret the goals for different protocols
5 To understand the Issues and challenges in providing QOS and security in Ad hoc wireless Networks

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	ADHOC NETWORKS: INTRODUCTION, ISSUES IN AD HOC WIRELESS NETWORKS, AD HOC WIRELESS INTERNET.MAC PROTOCOLS FOR ADHOC WIRELESS NETWORKS: INTRODUCTION, ISSUES IN DESIGNING A MAC PROTOCOL FOR AD HOC WIRELESS NETWORKS, DESIGN GOALS OF A MAC PROTOCOL FOR AD HOC WIRELESS NETWORKS, CLASSIFICATION OF MAC PROTOCOLS. TEXT1	10	L1, L2,L4
2	Contention based MAC protocols with scheduling mechanism, MAC protocols that use directional antennas, Other MAC protocols. **ROUTING PROTOCOLS FOR ADHOC WIRELESS NETWORKS:** Introduction, Issues in designing a routing protocol for Ad hoc wireless Networks, Classification of routing protocols, Table drive routing protocol, On-demand routing protocol. Text1	10	L1, L2,L4,L5
3	**Hybrid routing protocol,** Routing protocols with effective flooding mechanisms, Hierarchical routing protocols, Power aware routing protocols. **TRANSPORT LAYER PROTOCOLS FOR ADHOC WIRELESS NETWORKS:** Introduction, Issues in designing a transport layer protocol for Ad hoc wireless Networks, Design goals of a transport layer protocol for Ad hoc wireless Networks, Classification of transport layer solutions, TCP over Ad hoc wireless Networks, Other transport layer protocols for Ad hoc wireless Networks. Text1	10	L1,L2,L3,L4,L5
4	TRANSPORT LAYER PROTOCOLS FOR AD HOC WIRELESS NETWORKS: Introduction, Issues in designing a transport layer protocol for Ad hoc wireless Networks, Design goals of a transport layer protocol for Ad hoc wireless	11	L1,L4,L5

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	Networks.		
5	**QUALITY OF SERVICE IN ADHOC WIRELESS NETWORKS:** Introduction, Issues and challenges in providing QoS in Ad hoc wireless Networks, Classification of QoS solutions, MAC layer solutions, network layer solutions. Text1 SECURITY: Security in wireless Ad hoc wireless Networks, Network security requirements, Issues & challenges in security provisioning. QUALITY OF SERVICE IN AD HOC WIRELESS NETWORKS Introduction, Issues and challenges in providing QoS in Ad hoc wireless Networks, Classification of QoS solutions.	11	L1,L2,L6

Note 1: Unit 1 and Unit 5 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Define Adhoc network, identify issues related to different protocols for Adhoc network, like protocol , routing ,QoS and security aspects

CO2 Understand protocols require for Adhoc wireless network

CO3 Show implementation of routing protocol, scheduling mechanism and flooding mechanism

CO4 Analyse the routing protocol,MAC protocol, and Transport Protocol for Adhoc network

CO5 Interpret the design goals and evaluate the performance of different protocols for Adhoc wireless Network Click here to enter text.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO5,PO6,PO10

CO2 P01, PO2, PO5,PO8

CO3 P01, PO4,PO5,PO6

CO4 P01, PO2,PO3

CO5 PO2, PO5,PO6,PO9

Text Books.

1 Siva Ram Murthy & B. S. Manoj, "Ad hoc wireless Networks", 2nd edition, Pearson Education , 2004

Reference Text Books.

1 Ozan K. Tonguz and Gianguigi Ferrari, "Ad hoc wireless Networks", 2012 REPRINT, Wiley India, 2008
2 Xiuzhen Cheng, Xiao Hung, Ding-Zhu Du "**Ad hoc wireless Networking**", Kluwer Academic publishers, 2009

Web Links.

1 http:// nptel.ac.in/syllabus//

Subject Title : Data Structures using C++

Sub.Code: EC815 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 To become familiar with the Data representation and Addressing.
2 To understand Abstract Nature of Stacks and Queues.
3 To study various searching and sorting methods.
4 To understand Recursion and Linked lists.
5 To analyse different trees structures and Hashing.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Introduction:** Linear Lists, Formula based Representation, Linked Representation, Indirect Addressing, Simulating Pointers, Applications, Equivalence Classes, Convex Hull. TEXT 1	10	L1,L2,L3.
2	**Stacks**: The Abstract Data Type, Derived Classes and Inheritance, Formula Based Representation, Linked Representation, Applications. **Queues**: The Abstract Data Type, Formula Based Representation, Linked Representation, Applications TEXT 1	10	L1,L2,L3.
3	**Searching**: Search Techniques- Sequential Search, Binary Search, Fibonacci Search, Indexed sequential Search, Hashed Search. **Sorting**: Bubble sort, Insertion sort, Selection sort, quick sort, Shell sort, Bucket sort and Radix sort. TEXT 2	12	L1,L2,L3.
4	**Recursion**: introduction, Recurrence, use of stack in recursion, variants of recursion, execution of recursive calls, iteration vs recursion. **Linked Lists**: linked list, realization of linked lists, dynamic memory management, linked list abstract data type, circular linked list. TEXT 2	10	L1,L2,L3
5	**Search Trees**: Symbol Table, Optimal Binary Search tree, AVL tree **Hashing**: key terms, Hash Functions, Collision Resolution Strategies. TEXT 2	10	L1,L2,L3

Note 1: Unit 2 and Unit 3 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Outline the basic concepts of abstract data types.

CO2 Explain stacks, queues, recursion, hashing and linked lists.

CO3 Demonstrate the searching and sorting techniques.

CO4 Compare the program on data structure concepts.

CO5 Design the binary and AVL trees.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO3,PO4

CO2 PO1,PO2,PO3,PO4

CO3 PO1,PO2,PO3,PO4

CO4 PO1,PO2,PO3,PO4,PO11,PO12

CO5 PO1,PO2,PO3,PO4,PO11,PO12

Text Books.

1 Sahni, "Data Structures, Algorithms and Applications in C++", Edition, McGraw Hill International Edition, 2004

2 Varsha H. Patil, "Data Structures Using C++", edition, Oxford University Press, 2012

Reference Text Books.

1 Mark Allen Wiss, "Data Structures and Algorithms Analysis in C", 3rd Edition, Pearson, 2013

Web Links.

1 https://www.tutorialspoint.com/cplusplus/cpp_data_structures.htm

2 www.sourcetricks.com/p/data-structures-using-c.htm

3 www.cprogramming.com/algorithms-and-data-structures.html

Subject Title: VIRTUAL INSTRUMENTATION		
Subject Code: EC816	No. of Credits**:4= 4:0:0:0**	No. of lecture hours/week **:04**
Exam Duration : **03 Hours**	CIE +Assignment + SEE **= 45 + 5 + 50 =100**	Total No. of Contact Hours **:56**

Course Learning Objectives:

1. To understand the difference between conventional and graphical programming.
2. Differentiate between real and virtual instrumentation.
3. Introduce the basics of LAB VIEW and its programming.
4. Analyse the basics of data acquisition and learning it with Lab VIEW.
5. Provide the concept of interfacing peripherals.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy Level
1	**Fundamentals of Virtual Instrumentation:** Historical perspective, advantages, block diagram and architecture, data flow techniques, graphical programming in data flow, comparison with conventional programming.	10	L1, L2
2	**Software overview:** Lab VIEW, graphical user interface, controls and indicators, data types, data flow programming, editing, debugging and running VI, VIs and sub Vis.	**10**	**L1,L2**
3	**Programming structure:** FOR loops, WHILE loop, CASE structure, formula node, sequence structure, examples. **Introduction to arrays and clusters**: Array operations, Cluster functions, graphs and charts, local and global variables, examples.	**11**	**L1,L2,L3**
4	**File Input / output:** Introduction, file formats, file I/O functions, Sample VIs to demonstrate file WRITE and READ functions. **String handling:** Introduction, string functions, Lab-VIEW string formats, examples.	**11**	**L1,L2,L3**
5	**Basics of data acquisition:** Introduction, Classification of signals, Analog interfacing, connecting to board, Digital I/O.	**10**	**L1,L2,L3**

Note 1: Unit 3 and Unit 4 will have internal choice.

Note 2:Two assignments are evaluated for 5 marks:

Assignment – 1 from units 1 and 2.
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

1. Understand the architecture and Design front panel using Lab-VIEW.
2. Gain knowledge of debugging and running the Lab VIEW .

3. Understand the importance of FOR , WHILE AND CASE structure in Lab VIEW.
4. Demonstrate the file WRITE and READ functions.
5. Get the basic knowledge of data acquisition.

Cos	**Mapping with POs**
CO1	PO1, PO2
CO2	PO2, PO4
CO3	PO2, PO4, PO12
CO4	PO2, PO4, PO12
CO5	PO2, PO4, PO12

Text Books:

1. Sanjay Gupta, Joseph John, "Virtual instrumentation using Lab-VIEW*", 2nd* Edition, McGraw- Hill International edition, 2010, ISBN: 978-0070700284.

Reference Books:

1. Jovitha Jerome , "Virtual Instrumentation using LABVIEW", PHI , 2011
2. Lisa K. Wills, "Lab-VIEW for everyone", 4th Edition, Prentice hall India, 2008, ISBN: 978-0132681940.

Sub Title : SEMINAR		
Sub Code:ECS82	**No. of Credits:02=0 :0 :10 (L-T-P)**	**CIE + SEE = 50+0 =50**

The seminar should be on any topic having relevance with Electronics and Communication Engineering. The same should be decided by the student and concerned teacher. Seminar work shall be in the form of report to be submitted by the student at the end of the semester. The candidate will deliver a talk on the topic for half an hour and assessment will be made by two internal examiners appointed by Department UG Programme Committee, one of them will be guide. Usually the seminars should be related to dissertation topics. Student should submit report based on his study and is required to make presentation for evaluation

Sub Title : PROJECT WORK		
Sub Code:ECP83	**No. of Credits:10=0 :0 :10 (L-T-P)**	
Exam Duration :03 Hour	**CIE + SEE = 50+50 =100**	**Total No. of Contact Hours : 03**

A student is required to carry out elaborated project work. The project may be either design and fabrication work or a simulation of a problem on a computer. At the end of the semester student will be required to submit a detailed report of literature survey, design problem formulation, work plan and work done and will defend his/her work carried out before the examiners at the time of final evaluation.

Subject Title : Cryptography

Sub.Code: ECE01 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 To impart the basic concepts of network security and classical encryption, number theory, stream ciphers, block ciphers and authentication
2 To interpret the cryptographic algorithms like stream ciphers and block ciphers using classical encryption techniques
3 To apply the concept of classical encryption techniques to stream ciphers and block ciphers
4 To analyze the stream ciphers, block ciphers and authentication functions
5 To design the stream ciphers, block ciphers and authentication functions

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Introduction:** Services, mechanisms and attacks, OSI security architecture, Model for network security. **Symmetric ciphers:** Symmetric Cipher Model, Substitution Techniques: Caesar Cipher, Mono Alphabetic Cipher, Playfair Cipher, Hill Cipher, polyalphabetic Cipher and One-Time Pad (OTP). Transposition Techniques, Rotor Machines, Steganography. TEXT 1 and TEXT 1	11	L1,L2
2	**Finite Fields:** Groups, Rings, Fields. Modular Arithmetic: Divisors, properties of modulo operator, modular arithmetic operations and properties. Euclid's Algorithm, Greatest Common Divisor (GCD), finding GCD. Finite Fields of the form GF (p): Finite fields of order p, finding multiplicative inverse in GF (p). TEXT 1	11	L1,L2
3	**Private Key Encryption:** Simplified DES, Block Cipher Principles, Data encryption standard (DES), Strength of DES, Block Cipher Design Principles and Block Cipher Modes of Operation, Evaluation Criteria for Advanced Encryption Standard, The AES Cipher. TEXT 1	10	L2,L3,L4
4	**Public Key Encryption:** Principles of Public-Key Cryptosystems, The RSA algorithm. Key Management, Diffie - Hellman Key Exchange. TEXT 1	10	L2,L3,L4
5	**Authentication Functions and Hash Functions:** Authentication functions, message authentication codes, hash functions, security of Hash functions and MACs. TEXT 1	10	L2,L3,L4

Note 1: Unit 1 and Unit 2 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Define the basic concepts of network security, classical encryption, number theory, Private key, public key, authentication

CO2 Understand the structure of cryptographic algorithms and their applications.

CO3 Apply the concept of classical encryption techniques to existing standard algorithms.

CO4 Illustrate the significance of cryptographic algorithms and their applications.

CO5 Design the private key and public key, authentication functions for applications.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2,PO4,PO5,PO6,PO11, P12

CO2 P01, PO2,PO4,PO5,PO6,PO11, P12

CO3 P01, PO2,PO4,PO5,PO6,PO11, P12

CO4 P01, PO2,PO4,PO5,PO6,PO11, P12

CO5 P01, PO2,PO4,PO5,PO6,PO11, P12

Text Books.

1 William Stallings, "Cryptography and Network Security: Principles and Practice", Fifth Edition, Pearson, 2010

2 Enter name, "Book title", edition, publisher, year

3 Enter name, "Book title", edition, publisher, year

4 Enter name, "Book title", edition, publisher, year

5 Enter name, "Book title", edition, publisher, 2014

Reference Text Books.

1 Behrouz Forouzan, "Cryptography and Network Security", edition, TMH, 2007

2 Alfred J. Menezes, Paul C. Van Oorschot and Scott A. Vanstone, "Handbook of Applied Cryptography ", edition, CRC Press, Reprint 2001

3 Bruce Scheiner, "Applied cryptography: protocols, algorithms, and source code in C", 2nd edition, Wley India, 2008

4 Atul Kahate , "Cryptography and Network Security", 2nd edition, TMH, 2006

5 Enter name, "Book title", edition, publisher, year

Web Links.

1 http://www.nptel.ac.in/courses/106105031/

2 http://faculty.mu.edu.sa/public/uploads/1360993259.0858Cryptography%20and%20Network%20Security%20Principles%20and%20Practice,%205th%20Edition.pdf

3 Author Name, " Text Book title", Edition of the Text Book, Publisher Name, Year of the Publication

4 Author Name, " Text Book title", Edition of the Text Book, Publisher Name, Year of the Publication

5 Author Name, " Text Book title", Edition of the Text Book, Publisher Name, Year of the Publication

Subject Title : Automotive Safety Measurements

Sub.Code: ECE02 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 To understand overview of the automobile with emphasis on the basic operation of the engine
2 To understanding of electronic technology
3 To examine how electronics has been applied to the major systems
4 To understand various sensors and actuators and get some ideas and methods that may be used in the future
5 Understand the concepts of vehicle motion control.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Automotive Fundamentals Overview** – Four Stroke Cycle, Engine Control, Ignition System, Spark plug, Ignition Timing, Drive Train- Transmission, Brakes, Steering System. TEXT 1 and REFERENCE TEXT 1	9	L1
2	**Sensors** – Airflow rate sensor, Strain gauge MAP sensor, Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle angle sensor, Temperature sensor, Exhaust Gas Oxygen Sensor Knock Sensor. **Actuator** – Exhaust Gas Recirculation Actuator. TEXT 1 and REFERENCE TEXT 1	12	L1,L2
3	**Electronic Engine Control** – Concepts of an electronic engine control system, definition of general terms - Engine parameters, variables, Engine Performance terms –Power , BSFC, Torque, Volumetric efficiency, thermal efficiency, calibration, Effect of air/fuel ratio on performance, Effect of spark timing on performance, of EGR on performance Electronic fuel control system –open loop control, closed loop control. TEXT 1	12	L2,L3
4	**Vehicle Motion Control** – Cruise Control System-speed response curves, digital cruise control, Antilock Brake System (ABS), Electronic Suspension system, Electronic suspension control system. TEXT BOOK:1,REF. BOOK :1	9	L1,L3
5	**Safety systems -** Collision Avoidance Radar warning Systems, Low tire pressure warning system, navigation-navigation sensor, radio navigation signpost navigation, dead reckoning navigation, voice recognition cell phone dialing.	10	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	TEXT BOOK:1		

Note 1: Unit 2 and Unit 3 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Identify the different sensors, Actuators, Engine Control, Ignition System and Spark plug.

CO2 Summarize the concepts of an electronic engine control system, Cruise Control System.

CO3 Demonstrate the Engine Efficiency.

CO4 To analyse the concepts of an electronic engine control system, Vehicle Motion Control, Safety systems, sensors and actuators.

CO5 Relate Safety systems.

Course Outcomes Mapping with Programme Outcomes.

CO1 P01

CO2 P01

CO3 PO2, PO6, PO10

CO4 PO10, PO12

CO5 PO10, PO12

Text Books.

1 William Ribbons, "**Understanding Automotive Electronics**", Seventh Edition, Elsevier Publishing, 2012

Reference Text Books.

1 Robert Bosch GmbH, "**Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive**",Fifth Edition, Springer Fachmedien Wiesbaden Publishing, 2014

Sub Title : Semiconductor Fabrication		
Sub Code: ECE03	**No. of Credits:4=4 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : 3 Hours	**CIE +Assignment + SEE = 45 + 05 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. To be able to understand Scope of semiconductor Materials and Devices.
2. To be able to understand the Process of Crystal Growth.
3. To be able to understand the Photolithography and Etching.
4. To be able to classify the Diffusion and Ion Implantation.
5. To be able to understand the Film Deposition and Process Integration.

UNIT No	Syllabus Content	No of Hours
1	**Introduction to Semiconductor:** semiconductor Materials, Devices, Semiconductor process technology-key semiconductor technology, technology trends. Basic Fabrication Steps-oxidation, photolithography, etching, diffusion, Ion Implantation and metallization. **Text1**	10
2	**Crystal Growth:** Silicon crystal growth from the melt-starting material, czochralski technique, distribution dopant, effective segregation coefficient. Silicon float zone process. GaAs crystal growth techniques- starting materials, crystal growth techniques. Material characterization- wafer shaping, crystal characterization. **Silicon Oxidation:** Thermal oxidation process-kinetics of growth, thin oxide growth. Impurity redistribution during oxidation, Masking properties of silicon dioxide, oxide quality, oxide thickness characterization. **Text1**	10
3	**Photolithography and Etching:** Optical Lithography- the clean room, exposure tools, masks, photo resist, pattern transfer and resolution enhancement technique. **Etching:** Wet chemical etching-Si etching, Silicon dioxide etching, silicon Nitride and poly silicon etching, Aluminum etching and GaAs etching. Dry etching- Plasma Fundamentals, Etch mechanism, plasma diagnostics, and reactive plasma etching technique. **Text1**	10
4	**Diffusion and Ion Implantation:** Basic Diffusion Process- Diffusion Equation, Diffusion profiles. Extrinsic Diffusion and Lateral diffusion. **Introduction Ion Implantation:** Range of Implanted Ions- Ion Distribution, Ion Stopping, Ion Channeling. Implant Damage and Annealing- Implant Damage, Annealing. Implantation Related Processes- Multiple Implantation and Masking. **Text1**	11
5	**Film Deposition and Process Integration:** Epitaxial Growth Techniques- Chemical Vapor Deposition. Structures and Defects in Epitaxial Layers, Dielectric Deposition- Si Dioxide, Si Nitride. Poly silicon Deposition. Metallization- Physical Vapor Deposition and Aluminum Metallization and copper Metallization. **Process Integration:** The Integrated Circuit Resistor, Integrated Circuit Capacitor, Integrated Circuit Inductor and Bipolar Technology. **Text1**	11

Note 1: Unit 3 and Unit 4 will have internal choice.

Note 2: Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2

Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1: Identify the Semiconductor Materials.
CO2: Ability to interpret Fabrication Steps.
CO3: Creation of semiconductor devices
CO4: Ability to Compare the types of Diffusion and Ion Implantation.
CO5: Create the Integrated Circuit.
CO6: Ability to Conclude the best methods of Film Deposition and Process Integration

Cos	Mapping with POs
CO1	PO5,PO7,PO8
CO2	PO7,PO8,PO10
CO3	PO5,PO8,PO12
CO4	PO5,PO9,PO11
CO5	PO9,PO11,PO12
CO6	PO5,PO9,PO11, PO12

TEXT BOOK:

1. Gary S. May, Simon M. Sze, **"Fundamentals of Semiconductor Fabrication"** Wiley, 1st Edition, 2003.
2. Gary S. May, Costas J S, **"Fundamentals of Semiconductor Manufacturing and Process Control**" Wiley IEEE Press, 1st Edition, 2006.

REFERENCE BOOKS/WEBLINKS:

1. Anderson, Anderson" **Fundamentals of Semiconductor Devices**" McGraw-Hill Education, Indian Edition 2013.

Subject Title : Wireless Sensor Network

Sub.Code: ECE04 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 Students will be able to describe the unique issues in sensor networks.
2 Students will be able to describe current technology trends for the implementation and deployment of wireless sensor networks.
3 Students will be able to discuss the challenges in designing MAC, routing and transport protocols for wireless sensor networks.
4 Interpret the goals for different protocols
5 Students will be able to describe and implement protocols

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	Introduction: Unique Constraints and Challenges, Advantages of Sensor Networks, Energy advantage, Detection advantage, Sensor Network Applications, Habitat monitoring, Wildlife conservation through autonomous, non-intrusive sensing, Tracking chemical plumes, Ad hoc, just-in-time deployment mitigating disasters, Smart transportation: networked sensors making roads safer and less congested, Collaborative Processing.. TEXT1	10	L1, L2,L4
2	**Canonical Problem: Localization and Tracking,** A Tracking Scenario, *Sensing Model, Collaborative Localization, Bayesian State Estimation,* Distributed Representation and Inference of States: *Impact of Choice of Representation, Design consideration in Distributed Tracking,* Tracking Multiple Objects: *State-Space Decomposition, Data Association,* Sensor Models, Performance Comparison and Metrics , TEXT 1	10	L1, L2,L4,L5
3	Networking Sensors: Key Assumptions, Medium Access Control, General Issues, Geographic, Energy-Aware Routing: Unicast Geographic Routing, Routing on a Curve, Energy-Minimizing Broadcast, Energy-Aware Routing to a Region, Attribute-Based Routing. **Infrastructure Establishment:** Topology Control, Clustering, Time Synchronization, Localization and Localization Services, **Sensor Tasking and Control :**Task-Driven Sensing ,Roles of Sensor Nodes and Utilities Information-Based Sensor Tasking Sensor Selection IDSQ: Information-Driven Sensor Querying ,Cluster Leader–Based Protocol ,Sensor Tasking in Tracking Relations TEXT 1	13	L1,L2,L3,L4,L5
4	Sensor Network Databases: Sensor Network Databases,	10	L1,L4,L5

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	Sensor Database Challenges, Querying The Physical Environment, Query Interfaces, Cougar sensor database and abstract data types, Probabilistic queries, High-level Database Organization, In- Network Aggregation, Query propagation and aggregation, Tiny DB query processing, Query processing scheduling and optimization, Data-Centric Storage, Data Indices and Range Queries, One-dimensional indices, Multidimensional indices for orthogonal range searching, Non-orthogonal range searching, Distributed Hierarchical aggregation, Multi-resolution, Partitioning, Fractional cascading, Locality preserving hashing, Temporal Data, Data aging, Indexing motion data. TEXT 1		
5	Sensor Network Platforms: Sensor Node Hardware, Sensor Network Programming Challenges, Node-Level Software Platforms, Node-Level Simulators, Programming Beyond Individual Nodes: State-Centric Programming, and Tools Applications and Future Directions: Emerging Applications, Future Research Directions TEXT 1	08	L1,L2,L6

Note 1: Unit 1 and Unit 3 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Define WSN, identify issues related to different protocols for WSN

CO2 Understand protocols require for Wireless Sensor Network

CO3 Explore current sensor technologies through algorithms, protocols, and applications

CO4 Analyse routing ,tracking problems, data base requirement and programing challenges

CO5 Interpret the design goals consideration tracking and evaluate the performance of different protocols for wireless Sensor Network Click here to enter text.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO5,PO6,PO10

CO2 P01, PO2, PO5,PO8

CO3 P01, PO4,PO5,PO6

CO4 P01, PO2,PO3

CO5 PO2, PO5,PO6,PO9

Text Books.

1 Feng Zhao, Leonidas Guibas, "Wireless Sensor Networks, An Information Processing Approach", Elsevier, 2004

Reference Text Books.

1 Kazem Sohrabi,Daniel Minoli.Taieb Znati "Wireless Sensor Networks", Wiley Inter science, Wiley India, 2007

2

Web Links.

1 https://onlinecourses.nptel.ac.in/noc17_cs07

Subject Title : Mobile Communication

Sub.Code: ECE05 No. of Credits:04=04:0:0 (L - T – P) No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:52

Course Learning Objectives:

1 Able to understand the basics of wireless communication used for mobile telephony.
2 Able to understand basic methodologies of cellular system design.
3 Able to remember components and characteristics of 2.5G network, 3G network architecture.
4 Able to understand Spread Spectrum communication and CDMA technology
5 Able to remember characteristics of emerging wireless technologies

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	Evolution of wireless communication system: History of wireless communication, advantages and disadvantages of wireless communications ,wireless network generations, comparison of wireless systems, evolution to next generation networks, application of wireless communications, potential market areas. TEXT 1Click here to enter text.	10	L1, L2
2	Principles of cellular Communication: Cellular terminologies, cell structure and cluster, frequency reuse concept, cluster size and system capacity method of locating co channel cells, frequency reuse distance, co- channel interference and reduction methods, A Basic Cellular system: Limitations of conventional mobile telephone system, components of cellular system, operation of cellular system. TEXT 1	10	L1, L2
3	Global System for Mobile(GSM): GSM Network architecture, Signalling protocol Architecture, identifies in GSM system, GSM channels, frame structure, speech coding, authentication and security in GSM, services, TEXT1	10	L1,L2
4	CDMA digital cellular standards (IS 95): General model of Spread spectrum digital communication system, Direct sequence Spread Spectrum, Frequency hopping Spread Spectrum, Architecture of CDMA system. 3G Digital cellular Technology: 2.5G TDMA evolution, GPRS Technology, EDGE Technology, UMTS Technology-CDMA: Comparison of W-CDMA and IS 95.TEXT1	11	L1,L2
5	Emerging wireless Network Technologies: IEEE.802.11 technology, ETSI Hyper LAN Technology, IEEE.802.15 WPAN technology, IEEE.802.16 WMAN technology, Mobile AD-HOC network(MANETS), Wireless Sensor Networks (WSNs), Security requirements of wireless Networks, IEEE.802.21 standard-An	11	L1,L2

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	overview, Interoperability of Wireless Networks.TEXT1		

Note 1: Unit4and Unit5will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes:

CO1 Identify the telecommunication system and networks system, 3G cellular system components; list the components of wireless cellular network and different frequency band used in GSM and CDMA

CO2 Explain cellular systems, list the characteristics of 3G wireless mobile systems and network security

CO3 Explain the architecture of 3G and network Systems and the operation needed for call setup and call release in GSM and TDMA system and concept of CDMA,

CO4 Illustrate the cellular concept, cell sectoring and cell splitting, mobility management, CDMA channel concept, GSM frame concept ,,

CO5 Discuss characteristics of Emerging wireless Network Technologies

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2,PO5, P12

CO2 PO2, PO5, P12

CO3 PO2, PO5, P12

CO4 PO2, PO5, P12

CO5 PO2, PO5, P12

Text Books.

1 T L Singal, "Wireless Communications: , Tata McGraw-Hill Education , Delmar Cengage Learning,2010

Reference Text Books.

1 Garry J Mullet, "Introduction to Telecommunication Systems and Networks", India Edition, Delmar Cengage Learning, 2007

2 Upena Dalal, "Wireless communication", Oxford Higher Education, 6th impression,2013

Web Links.

1 http://www.nptel.ac.in /courses/117102062/

Dr. Ambedkar Institute of Technology
Electronics and communication Department

The enclosed documents are valid and verified.

HOD

ECE Department

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SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2018 Batch)

III Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing/ Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	BC	18MA31	Transforms & Applications	MAT	02	02	--	03	050	050	100	03
2	PC	18EC31	Electronics devices	EC	04	--	--	03	050	050	100	04
3	PC	18EC32	Digital System Design	EC	04	--	--	03	050	050	100	04
4	PC	18EC33	Network Theory	EC	04	--	--	03	050	050	100	04
5	PC	18EC34	Engineering Statistics	EC	03	--	--	03	050	050	100	03
6	PC	18EC35	Power Electronics & Instrumentation	EC	03	--	--	03	050	050	100	03
7	PC	18ECL36	Electronic Devices & Instrumentation Laboratory	EC	--	--	02	03	050	050	100	01
8	PC	18ECL37	Digital System Design Laboratory	EC	--	--	02	03	050	050	100	01
9	HS	18HS31/32	Constitution of India Professional Ethics and Cyber law /Environmental Studies	HS	01	--	--	02	050	050	100	01
10	MC	18HS33	Soft skills (MC)	HS	04	--	--	03	050	---	050	00
Total					**25**	**02**	**04**	**29**	**500**	**450**	**950**	**24**

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

11.	MC	18MAD41	Advance Mathematics - I	MAT	02	02	--	03	50	--	--	00

a.) The mandatory non – credit courses Advance Mathematics I and II prescribed at III and IV semesters respectively, to lateral entry Diploma holders admitted to III semester of BE programs shall compulsorily be registered during respective semesters to complete all the formalities of the course and appear for SEE examination.

b.) The mandatory non – credit courses Basic Engineering Mathematics I and II, prescribed to lateral entrant Diploma holders admitted to III and IV semester of BE programs, are to be completed to secure eligibility to VII semester. However, they are not considered for vertical progression from II year to III year of the programme but considered as head of passing along with credit courses of the programme to eligibility to VII semester.

Subject Title : Electronics Devices

Sub.Code: 18EC32 | No. of Credits:04=2:2:0 (L - T – P) | No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs | CIE+Assignment +SEE=45+5+50=100 | Total No.of Contact Hours:52

Course Learning Objectives: The student should be able to:

1 Understand the basics of semiconductor physics and electronic devices.

2 Describe the mathematical models BJTs and FETs along with the constructional details

3 Understand the construction and working principles of MOSFET

4 Understand the construction and working principles of optoelectronic and high power devices and circuits

5 Understand the fabrication process of semiconductor devices and CMOS process integration

Unit No	Syllabus Contents	No. of Hours	Blooms Taxnomy level.
1	Semiconductor and p-n Junctions Bonding forces in solids, Energy bands, Metals, Semiconductors and Insulators, Direct and Indirect semiconductors, Electrons and Holes, Intrinsic and Extrinsic materials, Conductivity and Mobility, Drift and Resistance, Effects of temperature and doping on mobility, Hall Effect. Forward and Reverse biased junctions-Qualitative description of Current flow at a junction, reverse bias, Reverse bias breakdown- Zener breakdown, avalanche breakdown, Rectifiers, Breakdown diode, Varactor diode.(Text 1)	10	L1,L2
2	Bipolar Junction Transistor Fundamentals of BJT operation, Amplification with BJTS, BJT Fabrication, The coupled Diode model (Ebers-Moll Model), Switching operation of a transistor, Cutoff, saturation, switching cycle, specifications, Drift in the base region, Base narrowing, Avalanche breakdown, Base Resistance and Emitter crowding, Capacitance and Charging times(hybrid-pi model), L1,L2 Heterojunction Bipolar Transistor. (Text 1).	11	L1,L2

Unit No	Syllabus Contents	No. of Hours	Blooms Taxnomy level.
3	Field Effect Transistors Basic pn JFET Operation, MESFET operation, MOSFET, Two terminal MOS structure- Energy band diagram, Depletion layer thickness, Work Function Difference, Flat band Voltage, Threshold Voltage. Ideal Capacitance – Voltage Characteristics and Frequency Effects, Basic MOSFET Operation- MOSFET structure, Current-Voltage Characteristics, Small Signal Equivalent Circuit and frequency limitation. (Text 2).	11	L1,L2
4	Optoelectronic Devices Photodiodes: Current and Voltage in an Illuminated Junction, Solar Cells, Photodetectors. Light Emitting Diode: Light Emitting materials. High Power devices: The P-N-P-N Diode, Insulated Gate Bipolar Transistor. Nanoelectronic Devices: Zero Dimensional Quantum Dots, One Dimensional Quantum Wires, Two Dimensional Layered crystals, Spintronic memory, Nanoelectronic Resistive memory.(Text 1)	10	L1,L2
5	Fabrication of p-n junctions-Thermal Oxidation, Diffusion, Rapid Thermal Processing, Ion implantation, chemical vapour deposition, photolithography, Etching, Metallization. Integrated Circuits: Background, Evolution of ICs: CMOS Process Integration, Integration of Other Circuit Elements. (Text 1).	10	L1,L2,L3.

Note 1: Each Unit will have Internal Choice

Course Outcomes: After the completion of the Course the student should be able to :

CO1 Understand the principles of semiconductor Physics.

CO2 Understand the principles and characteristics of different types of semiconductor devices

CO3 Understand the fabrication process of semiconductor devices

CO4 Understand and utilize the mathematical models of semiconductor junctions and MOS transistors for circuits and systems.

CO5 Differentiate the semiconductor devices based on its usage and applications

Course Outcomes Mapping with Programme Outcomes.

CO1	PO1,PO2,PO3,PO5
CO2	PO1,PO2,PO5
CO3	PO1,PO2,PO3
CO4	PO1,PO2,PO3
CO5	PO1,PO2,PO5

Text Books.

1. Ben.G.Streetman, Sanjay Kumar Banergee, "Solid State Electronic Devices", 7th edition, Pearson Education, 2016
2. Donald A Neamen, Dhrubes Biswas, "Semiconductor Physics and Devices", 4th edition, Semiconductor Physics and Devices, 2012

Reference Text Books.

1. S.M.Sze, Kwok K. Ng, "Physics of Semiconductor Devices", 3rd edition, Wiley, 2018
2. A.Bar-Lev, ""Semiconductor and Electronic Devices", 3rd edition, PHI, 1993
3. Enter author name, Christos C. Halkias "Book title", edition, publisher, year
4. Choose an item., "Choose an item.", Choose an item., Choose an item., Choose an item.
5. Choose an item., "Choose an item.", Choose an item., Choose an item., Choose an item.
6. Choose an item., "Choose an item.", Choose an item., Choose an item., Choose an item.

Web Links.

1. www.nptel.in
2. https://www.youtube.com/watch?v=w8Dq8blTmSA

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
Dr. AMBEDKAR INSTITUTE OF TECHNOLOGY, BENGALURU-560 056
(An Autonomous Institution Affiliated To VTU, Belagavi)
Department Committees For the Academic year 2018-19 to 2020-21

Subject Title : DIGITAL SYSTEM DESIGN

Sub.Code: 18EC33	No. of Credits:03=2:2:0 (L - T – P)	No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs	CIE+Assignment +SEE=45+5+50=100	Total No.of Contact Hours:39

Course Learning Objectives: The student should be able to:

1 Illustrate simplification of Algebraic equations using Karnaugh Maps and Quine Techniques.
2 Design Decoders, Encoders, Digital Multiplexer, Adders, Subtractors and Binary Comparators.
3 Describe Latches and Flip-flops, Registers and Counters. Analyze Mealy and Moore Models.
4 Develop state diagrams Synchronous Sequential Circuits.
5 To provide the basic knowledge about VHDL and its use.

Unit No	Syllabus Contents	No. of Hours	Blooms Taxnomy level.
1	**Principles of combination logic**: Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don't care terms) Simplifying Max term equations. (Text 1, Chapter 3).	07	L1,L2,L3.
2	**Analysis and design of combinational logic:** Decoders, Encoders, Digital multiplexers, Adders and subtractors, Look ahead carry, Binary comparators.(Text 1, Chapter 4).	09	L1,L2,L3,L4
3	**Flip-Flops and its Applications:** Basic Bistable elements, Latches, The master-slave flip-flops (pulse-triggered flip-flops): SR flip-flops, JK flip- flops, Characteristic equations, Registers, binary ripple counters, synchronous binary counters. Text 2, Chapter 6)	07	L1,L2,L3.
4	**Sequential Circuit Design:** Design of a synchronous counter, Design of a synchronous mod-n counter using clocked JK, D, T and SR flip-flops. Mealy and Moore models, State machine notation, Construction of state diagrams. (Text 2,1 Chapter 6)	07	L1,L2,L3.

Unit No	Syllabus Contents	No. of Hours	Blooms Taxnomy level.
5	**HDL:** A brief history of HDL, Structure of HDL Module, Operators, Data types, Types of Descriptions (only VHDL), Simulation and Synthesis, brief comparison of VHDL and Verilog. Data-Flow Descriptions: Structure of data flow description (only VHDL). (Text 3 Chapter 1,2)	09	L1,L2,L3.

Note 1: Each Unit will have Internal Choice

Note 2: Five experiments are to be conducted and evaluated for 5 marks

Course Outcomes: After the completion of the Course the student should be able to :

CO1 Develop simplified switching equation using Karnaugh Maps .

CO2 Explain the operation of decoders, encoders, multiplexers, demultiplexers, adders, subtractors and comparators.

CO3 Explain the working of Latches and Flip Flops (SR,D,T and JK).

CO4 Design Synchronous/Asynchronous Counters and Shift registers using FlipFlops.

CO5 Develop Mealy/Moore Models and state diagrams for the given clocked sequential circuits.

CO6 Describe the structure of HDL module and data-flow description.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO3,PO5

CO2 PO1,PO2,PO5

CO3 PO1,PO2,PO3

CO4 PO1,PO2,PO3

CO5 PO1,PO2,PO5

Text Books.

1. Digital Logic Applications and Design, John M Yarbrough, Thomson Learning, 2001. ISBN 981-240-062-1.
2. Donald D. Givone, ―Digital Principles and Design‖, McGraw Hill, 2002. ISBN 978-0-07-052906-9.

3. HDL Programming (VHDL and Verilog)-Nazeih M.Botros-John Weily India Pvt. Ltd. 2008.

Reference Books:

1. D. P. Kothari and J. S Dhillon, ―Digital Circuits and Design‖, Pearson, 2016, ISBN:9789332543539.
2. Morris Mano, ―Digital Design‖, Prentice Hall of India, Third Edition.
3. Charles H Roth, Jr., ―Fundamentals of Logic Design, Cengage Learning.
4. 4. K. A. Navas, ―Electronics Lab Manual‖, Volume I, PHI, 5th Edition, 2015

ISBN:9788120351424.

Subject Title : Network Theory

Sub.Code: 18EC34 | No. of Credits:04=3:1:0 (L - T – P) | No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs | CIE+Assignment +SEE=45+5+50=100 | Total No.of Contact Hours:52

Course Learning Objectives: The student should be able to:

1 Able to Understand and Analyze the basic concepts emphasizing Series and Parallel combination of passive and active Components, Source transformation and Source shifting Techniques. Able toy to apply the concept of Mesh and Nodal analysis techniques to analyze the Electrical networks
2 Able to Define the statements of circuit Theorems, and understand, analyze the network theorems to simplify the complicated electrical circuits..
3 Able to Understand and analyze the dynamic behaviour(DC Response) of electrical networks using initial and final conditions.
4 Able to Apply the Laplace Transforms to Electrical Circuits and Understand & analyze the mathematical model of electrical circuits with periodic and non periodic signals as inputs.
5 Able to Define various two port network parameters, Resonance and its applications.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Basic Circuit Concepts:** Ideal and Practical sources, Network reduction using Source transformations and Star Delta transformation, duality of networks, Loop and Nodal analysis with linearly dependent and independent sources for both DC and AC networks, Concepts of super node and super mesh analysis, Numerical examples. *TEXT 1 and TEXT 2.*	10	L1,L2,L3.
2	**Network Theorems:** Thevenin's Theorem, Norton's Theorem, Superposition Theorem, Reciprocity Theorem, Maximum Power transfer theorem. Numerical examples **Resonant Circuits**: Series Resonance & Parallel Resonance Circuits, Frequency Response of series and parallel circuits,Q factor and bandwidth. Numerical Examples.	10	L1,L2,L3

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	TEXT 2 and TEXT 1.		
3	**Transient Behavior and Initial Conditions:** Behavior of circuit elements under switching condition and their representation, Evaluations of initial and final conditions in RL, RC and RLC circuits only for DC excitations. *TEXT 1 and TEXT 2.*	12	L1,L2,L3.
4	**Laplace Transforms:** Introduction, Properties and theorems of Laplace Transforms, response of electrical circuits with and without initial conditions. *TEXT 2 and TEXT 1.*	10	L1,L2,L3.
5	**Two port network parameters:** Definitions of Z,Y,T and h-parameters, modeling of two port network parameters. *TEXT 2 and TEXT 1.*	10	L1,L2,L3.

Note 1: Each Unit will have Internal Choice

Note 2: Two assignments are to be evaluated for five marks.

Course Outcomes: After the completion of the Course the student should be able to :

CO1 Define and classify electrical elements, resonance, two port network parameters and also state the different network theorems.

CO2 Explain Loop, nodal analysis, Resonance, initial conditions and transient behavior, properties and theorems of Laplace Transforms. relation between network parameters and interconnection of networks.

CO3 Apply the source transformation, sifting, Laplace transforms and basic theorems to simplify the analysis of electrical Circuits.

CO4 Evaluate the dynamic behavior of Electrical networks using initial and final conditions.

CO5 Solve the given network using specified two port network parameter like Z or Y or T or h.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1, PO11, PO12

CO2 PO1, PO2, PO11, PO12

CO3 PO1, PO2, PO3, PO11, PO12

CO4 PO1, PO2, PO3, PO11, PO12

CO5 PO1, PO2, PO3, PO11, PO12

Text Books.

1 M.E. Van Valkenberg, "Network analysis", 3rd edition, Prentice Hall of india Publishers, 2000

2 Roy Choudhury, "Networks and systems", 2nd edition, New Age International Publications, 2006

3 Charles K Alexander and Mathew N O Sadiku, "Fundamentals of Electric Circuits", 3rd edition, Tata McGraw-Hill, 2009

Reference Text Books.

1 Hayt, Kemmerly and Durbin, "Engineering Circuit Analysis", 7th Edition, TMH, 2010.

2 J. David Irwin /R. Mark Nelms, "Basic Engineering Circuit Analysis", 8th Edition, John Wiley, 2006.

4 A. Sudhakar and Shyam Mohan S Pillai, "E circuits and Networks ", 5th Edition, MC Graw Hill Education, 2015.

5 Ravish R Singh, Electrical Networks", 2nd Edition, MC Graw Hill Education, 2009.

Web Links.

1 nptel.ac.in/courses/108102042/

2 gradestack.com/Circuit-Theory-and/Laplace...and.../19349-3926-40444-study-wtw

3 https://www.khanacademy.org/science/electrical-engineering/ee-circuit-analysis-topic

Subject Title : Engineering Statistics & Linear Algebra

Sub.Code: 18EC35 | No. of Credits:03=2:2:0 (L - T – P) | No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs. | CIE+Assignment +SEE=45+5+50=100 | Total No.of Contact Hours:39

Course Learning Objectives: The student should be able to:

1. Understand the meaning of Single and Multiple Random Variables, and extension to Random Processes. Familiarization with the concept of Vector spaces and orthogonality with a qualitative insight into applications in communications..

2. Analyze mathematically the quantitative parameters of Single and Multiple Random Variables as well as Random Processes.

3. Compute the quantitative parameters for functions of single and Multiple Random Variables and Processes. Compute the quantitative parameters for Matrices and Linear Transformations
4. Associate the concepts of Random Processes to examples that involve transmission through Filters.

Unit No	Syllabus Contents	No. of Hours	Blooms Taxnomy level.
1	**Single Random Variables:** Definition of random variables, cumulative distribution function continuous and discrete random variables; probability mass function, probability density functions and properties; Expectations, Characteristic functions, Functions of single Random Variables, Conditioned Random variables. Application exercises to Some special distributions: Uniform, Exponential, Laplace, Gaussian; Binomial, and Poisson distribution. (chapter 4 Text 1)	8	L1,L2,L3
2	**Multiple Random variables:** Concept, Two variable CDF and PDF, Two Variable expectations (Correlation, orthogonality, Independent), Two variable transformation, Two Gaussian Random variables, Sum of two independent Random Variables, Sum of IID Random Variables – Central limit Theorem and law of large numbers, Conditional joint Probabilities, Application exercises to Chi-square RV, Student-T RV, Cauchy and Rayleigh RVs. (chapter 5	8	L1,L2,L3

Unit No	Syllabus Contents	No. of Hours	Blooms Taxnomy level.
	Text 1)		
3	**Random Processes:** Ensemble, PDF, Independence, Expectations, Stationarity, Correlation Functions (ACF, CCF, Addition, and Multiplication), Ergodic Random Processes, Power Spectral Densities (Wiener Khinchin, Addition and Multiplication of RPs, Cross spectral densities), Linear Systems (output Mean, Cross correlation and Auto correlation of Input and output), Exercises with Noise. (chapter 6 Text 1)	8	L1,L2,L3
4	**Vector Spaces:** Vector spaces and Null subspaces, Rank and Row reduced form, Independence, Basis and dimension, Dimensions of the four subspaces, Rank-Nullity Theorem, Linear Transformations Orthogonality: Orthogonal Vectors and Subspaces, Projections and Least squares, Orthogonal Bases and Gram- Schmidt Orthogonalization procedure. (Refer chapters 2 and 3 Text 2)	8	L1,L2,L3
5	**Determinants:** Properties of Determinants, Permutations and Co-Factors. (Refer Chapter 4, Text 2) Eigenvalues and Eigen vectors: Review of Eigenvalues and Diagonalization of a Matrix, Special Matrices (Positive Definite, Symmetric) and their properties, Singular Value Decomposition. (Refer Chapter 5, Text 2)	7	L1,L2,L3

Note1: Each Unit will have Internal Choice

Course Outcomes: After the completion of the course the student should be able to:

CO1 Associate the concepts of statistics to Communication events and identify corresponding Random Variables and Random Processes in these events.

CO2 Analyse and model the Random events in typical communication events to extract quantitative statistical parameters.

CO3 Analyse and model typical signal sets in terms of a basis function set of Amplitude, phase and frequency.

CO4 Demonstrate by way of simulation or emulation the ease of analysis employing basis functions

CO5 Demonstrate by way of simulation or emulation the ease of analysis employing statistical representation.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO3,PO5

CO2 PO1,PO2,PO5

CO3 PO1,PO2,PO3

CO4 PO1,PO2,PO3

CO5 PO1,PO2,PO5

Text Books.

1 Richard H Williams, "Probability, Statistics and Random Processes for Engineers" Cengage Learning, 1st Edition, 2003, ISBN 13: 978-0-534-36888-3, ISBN 10: 0-534-36888-3.

2 Gilbert Strang, "Linear Algebra and its Applications", Cengage Learning, 4th Edition, 2006, ISBN 97809802327

Reference Text Books.

1 Hwei P. Hsu, "Theory and Problems of Probability, Random Variables, and Random Processes" Schaums Outline Series, McGraw Hill. ISBN 10: 0-07-030644-3.

2 K. N. Hari Bhat, K Anitha Sheela, Jayant Ganguly, "Probability Theory and Stochastic Processes for Engineers", Cengage Learning India, 2019, ISBN: Not in book

Subject Title : Power electronics and Instrumentation

Sub.Code: 18EC36 | No. of Credits:03=3:0:0 (L - T – P) | No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs | CIE+Assignment +SEE=45+5+50=100 | Total No.of Contact Hours:39

Course Learning Objectives: The student should be able to:

1 Study and analysis of thyristor circuits with different triggering conditions

2 Learn the applications of power devices in controlled rectifiers, converters.

3 Develop circuits for multirange Ammeters and Voltmeters, Multimeters.

4 Describe principle of operation of digital measuring instruments and Bridges.
.

5 Understand the operation of different Transducers.
.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	Introduction: History, Power Electronic Systems, Power Electronic Converters and Applications. Thyristors: Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-OFF mechanisms, Turn-OFF Methods: Natural and Forced Commutation – Class A and Class B types, Gate Trigger Circuit: Resistance Firing Circuit, Resistance capacitance firing circuit, Unijunction Transistor: Basic operation and UJT Firing Circuit. *TEXT 1*	09	L1,L2
2	Phase Controlled Converter: Control techniques, Single phase half wave and full wave controlled rectifier with resistive and inductive loads, effect of freewheeling diode. Choppers: Chopper Classification, Basic Chopper operation: step-down, step-up and step-up/down choppers. *TEXT 1*.	09	L1,L2,L3
3	Principles of Measurement: Static Characteristics, Error in Measurement, Types of Static Error.	07	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
	Voltmeters: Introduction, Multi range voltmeter, Loading. Ammeters: DC Ammeter, Multi-range Ammeter. Digital Voltmeter: Ramp Technique, Dual slope integrating Type DVM, Direct Compensation type and Successive Approximations type DVM. Text 2		
4	Digital Instruments: Introduction, Digital Multimeter, Digital frequency meters, Digital measurement of time. Signal Generators: Function generator, Frequency synthesizer, Oscilloscope. Bridges: Wheatstone's Bridge, AC Bridges-Capacitance and Inductance Comparison bridge, Maxwell's bridge, Wien's bridge. Text 2	07	L1,L2,L3.
5	Transducers: Introduction, Selecting a transducer, Electrical Transducer, Resistive Transducer, Resistive position Transducer, Resistance Wire Strain Gauges, Resistance Thermometer, Thermistor, LVDT, Instrumentation Amplifier using Transducer Bridge. Text 2	07	L1,L2,L3.

Note 1: Each Unit will have Internal Choice

Note 2: Two assignments are to be evaluated for five marks.

Course Outcomes: After the completion of the Course the student should be able to :

CO1 Build and test circuits using power devices such as SCR

CO2 Analyze and design controlled rectifier, DC to DC converters, DC to AC inverters.

CO3 Develop circuits for multirange Ammeters, Voltmeters.

CO4 Describe the principle of operation of Digital instruments

CO5 Use different transducers for measuring physical parameters.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1, PO11, PO12

CO2 PO1, PO2, PO11, PO12

CO3 PO1, PO2, PO3, PO11, PO12

CO4 PO1, PO2, PO3, PO11, PO12

CO5 PO1, PO2, PO3, PO11, PO12

Text Books.

1 M.D Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897

2 H. S. Kalsi, "Electronic Instrumentation", McGraw Hill, 3rd Edition, 2012, ISBN:9780070702066.

3 David A. Bell, "Electronic Instrumentation & Measurements", Oxford University Press PHI 2nd Edition, 2006, ISBN 81-203-2360-2.

Reference Text Books.

1. Mohammad H Rashid, Power Electronics, Circuits, Devices and Applications, 3rd/4th Edition, Pearson Education Inc, 2014, ISBN: 978-93-325-1844-5.
2.
2. L. Umanand, Power Electronics, Essentials and Applications, John Wiley India Pvt. Ltd, 2009.

ELECTRONIC DEVICES AND INSTRUMENTATION LABORATORY SEMESTER – III (EC/TC)			
Laboratory Code	**18ECL37**	**CIE Marks**	
Number of Lecture Hours/Week 03Hr	**Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	
RBT Level	**L1, L2, L3**	**Exam Hours**	**03**

Course objectives:

This laboratory course enables students to

- Understand the circuit schematic and its working
- Study the characteristics of different electronic devices
- Design and simple electronic circuits as per the specifications using discrete Electronic components.
- Familiarize with Sequel software which can be used for electronic circuit simulation.

Laboratory Experiments
PART A : Experiments using Discrete components
1. Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative)
2. Conduct experiment on Half wave rectifier and Full wave rectifier with and without filter and measure the ripple factor
3. Determine characteristics of Zener diode and design a Simple Zener voltage regulator to determine line and load regulation.
4. Design of RC coupled amplifier using BJT to determine
5. Conduct experiment on RC phase shift Oscillator using BJT
6. Conduct experiment on Hartley and Colpitts Oscillator using BJT.
7. Conduct experiment on Voltage series feedback amplifier

8. Conduct experiment on determine the transfer and drain characteristics of a JFET

PART-B : Simulation using SEQUEL

1. Design and verification of voltage follower , inverting amplifier and non-inverting amplifier using OP-AMP
2. Design and verification of Integrator and Differentiator using OP-AMP
3. Design and Simulation of Function generator to generate square wave and ramp signal using OP-AMP
4. Input, Output and Transfer characteristics of BJT Common emitter configuration and evaluation of parameters

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Understand the characteristics of various electronic devices and measurement of parameters.
- Design and test simple electronic circuits
- Use of circuit simulation software for the implementation and characterization of electronic circuits and devices.

Conduct of Practical Examination:

- All laboratory experiments are to be considered for practical examination.
- For examination one question from PART-A and one question from PART-B.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

Reference Books:

1. David A Bell, “Fundamentals of Electronic Devices and Circuits Lab Manual, 5th Edition, 2009, Oxford University Press.

Subject Title : Digital Design Lab

Sub.Code: 18ECL38 No. of Credits:2=0:2:2 (L - T – P) No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs CIE +SEE=50+50=100 Total No.of Contact Hours:39

Course Learning Objectives:

1 Enable the students to get practical experience in simplifying the logical expression and its realization using logic gates and its testing.
2 Ability to understand, design, Testing and Combinational logic circuits.
3 Ability to Understand to realize Combinational logic circuits using MSI IC's
4 Ability to Understand the Truth Table and Verifications of Flip-Flops
5 Ability to Design and Testing of Sequential Logic circuits such as Registers and Counters.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	Simplification, realization of Boolean expressions using logic gates.	3	L1, L2
2	Designing and testing of Binary to Gray code conversion and vice versa	3	L1,L2,L3.
3	MUX/DEMUX – use of 74153, 74139 for code converter and arithmetic circuits.	3	L1, L2, L3,L4
4	Use of Decoder chip (7447) to drive 7-Segment LED display and Priority encoder.	3	L1, L2, L3, L4
5	Designing and testing of Half/Full adder and Half/Full Subtractors using logic gates.	3	L1, L2
6	Realization of combinational logic circuits using 7483 and logic gates i. BCD to Excess-3 code conversion and vice versa. ii. Parallel adder/Subtractor.	3	L1,L2
7.	Designing and testing of One/Two bit comparator and study of 7485	3	L1,L2
8.	Truth table verification of Flip-Flops: SR, D, JK, MSJK and MST - type (Using logic gates)	3	L1,L2
9	Testing of 4 bit sequential circuit/ MOD – N counter(7490, 7493, 74190, 74192, 74193)	3	L1,L2
10	Designing and testing of 3 bit sequential circuit and MOD – N counter design (7476)	3	L1,L2
11	Shift Registers: SISO (Shift right), SIPO, PISO, PIPO, Shift left operations using 7495.	3	L1,L2
12	Designing and testing Ring counter/Johnson counter using 7495	3	L1,L2

Course Outcomes:

CO1 Demonstrates the truth table of various expressions and combinational circuits using logic gates.
CO2 Design, test and evaluate various combinational circuits such as adders, Subtracts, Multiplexers,

De-Multiplexers.

CO3 Construction of Flip-Flops and its truth table verification

CO4 Construction of Various applications of Sequential logic circuits.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO2, PO4, PO5, PO11, PO12

CO2 PO2, PO4, PO5, PO11, PO12

CO3 PO4, PO5, PO11, PO12

CO4 PO4, PO5, PO11, PO12

Text Books.

1 John M. Yarbrough, "**Digital Logic, Application & Design**", First Edition, Thomson , **2002**

2 Donald D. Givone, "**Digital Principles and Design**", 2nd edition, Tata Mcgraw Hill Education Pvt. , 2003

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2018 Batch)

IV Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1.	BC	18MA41	Probability, Numerical and Optimization Technique	MAT	02	02	--	04	050	050	100	03
2.	PC	18EC41	Analog Circuits	EC	04	--	--	04	050	050	100	04
3.	PC	18EC42	Principles of Communication Systems	EC	03	--	--	03	050	050	100	03
4.	PC	18EC43	Computer Organization and Architecture	EC	04	--	--	04	050	050	100	03
5.	PC	18EC44	Verilog HDL	EC	04	--	--	04	050	050	100	04
6.	PC	18EC45	Signals and Systems	EC	04	--	--	04	050	050	100	04
7.	PC	18ECL46	Analog Circuits and Communication Laboratory	EC	--	--	02	02	050	050	100	01
8.	PC	18ECL47	HDL Lab	EC	--	--	02	02	050	050	100	01
9.	CIV	18HS41/ 42	Constitution of India Professional Ethics and Cyber law/ Environmental Studies	HS/CIV	01	--	--	01	050	050	100	01
10.	MC	18HS43	Soft skills (NCMC)	HS	04	--	--	04	050	--	050	00
				Total	**26**	**02**	**04**	**32**	**500**	**450**	**950**	**24**

Course prescribed to lateral entry Diploma holders admitted to III semester of Engineering programs

11.	MC	18MAD41	Advance Mathematics - II	MAT	02	02	--	03	50	--	--	00

a.) The mandatory non – credit courses Advance Mathematics I and II prescribed at III and IV semesters respectively, to lateral entry Diploma holders admitted to III semester of BE programs shall compulsorily be registered during respective semesters to complete all the formalities of the course and appear for SEE examination.

b.) The mandatory non – credit courses Basic Engineering Mathematics I and II, prescribed to lateral entrant Diploma holders admitted to III and IV semester of BE programs, are to be completed to secure eligibility to VII semester. However, they are not considered for vertical progression from II year to III year of the programme but considered as head of passing along with credit courses of the programme to eligibility to VII semester.

Subject Title : Analog Circuits

Sub.Code: 18EC42 | No. of Credits:04=2:2:0 (L - T – P) | No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs | CIE+Assignment +SEE=45+5+50=100 | Total No.of Contact Hours:52

Course Learning Objectives: The student should be able to:

1 Explain various BJT parameters, connections and configurations.

2 Design and demonstrate the diode circuits and transistor amplifiers

3 Construct frequency response of FET amplifiers at various frequencies

4 Analyze Power amplifier circuits in different modes of operation and Feed back amplifier circuits

5 Construct and analysis of filter circuits

Unit No	Syllabus Contents	No. of Hours	Blooms Taxnomy level.
1	BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias, Collector to base feedback resistor, constant current source, Small signal operation and Modeling: Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, DC quantities, The hybrid Π model. MOSFETs: Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor, Constant current source. Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, Hybrid Π model.[Text 1]	11	L1,L2,L3
2	MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance RS, CG amplifier, Source follower and comparisons. MOSFET internal capacitances and High frequency model: The gate capacitive effect, Junction capacitances, High frequency model, Unity L1, L2, L3 gain frequency Frequency response of the CS amplifier: The three frequency bands, high frequency response, Low	11	L1,L2,L3

Unit No	Syllabus Contents	No. of Hours	Blooms Taxnomy level.
	frequency response. [Text 1]		
3	Feedback Amplifier: General feedback structure, Properties of negative feedback, Basic feedback topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative analysis). Power Amplifiers: Introduction, Classification, Class A operation, Transfer Characteristics, Signal Waveforms, Power Dissipation, Power Conversion efficiency, Transformer Coupled Power Amplifiers, Class B transformer coupled amplifier, Class B output stage, Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB – Operation, Output Resistance, Class C tuned Amplifier. Oscillators: FET based Phase shift oscillator, LC and Crystal Oscillators [Text 1]	10	L1,L2,L3
4	Op-Amp with Negative Feedback and general applications Inverting and Non inverting Amplifiers – Closed Loop voltage gain, Input impedance, Output impedance, Bandwidth, Total output offset voltage with feedback. DC and AC Amplifiers, Summing, Scaling and Averaging Amplifiers, Instrumentation amplifier, Comparators, Zero Crossing Detector, Schmitt trigger. [Text 2]	10	L1,L2,L3
5	Op-Amp Circuits: DAC - Weighted resistor and R-2R ladder, ADC Successive approximation type, Peak detector, Sample and hold circuit, Precision rectifiers-half and full wave. First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters and All-pass filters. Square and Triangular Wave Generators. Voltage Controlled Oscillator. 555 Timer applications: Monostable and Astable Multivibrators. [Text 2]	10	L1,L2,L3.

Note 1: Each Unit will have Internal Choice

Course Outcomes: After the completion of the Course the student should be able to :

CO1 Understand the characteristics of BJTs and FETs

CO2 Design and analyze BJT and FET amplifier circuits

CO3 Understand the fabrication process of semiconductor devices

CO4 Understand the functioning of linear ICs and design of Linear IC based circuits

CO5 Understand and design of the Filter circuits.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO3,PO5

CO2 PO1,PO2,PO5

CO3 PO1,PO2,PO3

CO4 PO1,PO2,PO3

CO5 PO1,PO2,PO5

Text Books.

1 Microelectronic Circuits, Theory and Applications, "Microelectronic Circuits, Theory and Applications", 6th edition, Oxford, 2015.

2 Ramakant A Gayakwad, "Op-Amps and Linear Integrated Circuits", 4th edition, Pearson Education, 2000

Reference Text Books.

1 Robert L Boylestad and Louis Nashelsky, "Electronic Devices and Circuit Theory s", 11th edition, Pearson Education, 2013

2 Behzad Razavi, "Fundamentals of Microelectronics", 2nd edition, John Weily, 2015.

3 Enter author name, Christos C. Halkias "Book title", edition, publisher, year

4 Choose an item., "Choose an item.", Choose an item., Choose an item., Choose an item.

5 Choose an item., "Choose an item.", Choose an item., Choose an item., Choose an item.

6 Choose an item., "Choose an item.", Choose an item., Choose an item., Choose an item.

Web Links.

1 www.nptel.in

2 https://www.youtube.com/watch?v=w8Dq8blTmSA

Subject Title : Principles of Communication Systems

Sub.Code: 18EC43 | No. of Credits:03=3:0:0 (L - T – P) | No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs | CIE+Assignment +SEE=45+5+50=100 | Total No.of Contact Hours:39

Course Learning Objectives: The student should be able to:

1 Understand the concepts of AM, FM, Low pass sampling and Quantization as process.
2 Analyse and mathematically model AM, FM, white noise and the process of sampling, quantization, and encoding.
3 Compute the crucial performance parameter SNR in the presence of AWGN.
4 Associate the concepts of AM, FM in thematic examples.
5 Understand and Analyze the different building blocks in digital electronics using logic gates and implement simple logic function using basic universal gates.

Unit No	Syllabus Contents	No .of Hours	Blooms Taxnomy level.
1	**Amplitude Modulation:** Introduction, Amplitude Modulation: Time & Frequency Domain description, Switching modulator, Envelop detector**.** **Double Side Band-Suppressed Carrier Modulation:** Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing. **Single Side–Band And Vestigial Sideband Methods Of Modulation**: SSB Modulation, VSB Modulation, Frequency Translation, Frequency- Division Multiplexing, Theme Example: VSB Transmission of Analog and Digital Television. (Chapter 3 of Text).	09	L1, L2, L3.
2	**Angle Modulation:** Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals, FM Stereo Multiplexing, Phase–Locked Loop: Nonlinear model of PLL, Linear	08	L1, L2, L3

Unit No	Syllabus Contents	No .of Hours	Blooms Taxnomy level.
	model of PLL, Nonlinear Effects in FM Systems. The Superheterodyne Receiver (refer Chapter 4 of Text).		
3	**Noise:** Review of Random Processes, Mean, Correlation and Covariance function, Properties of autocorrelation and, Cross– correlation functions. Shot Noise, Thermal noise, White Noise, Noise Equivalent Bandwidth (refer Chapter 5 of Text).	07	L1, L2, L3.
4	**Noise In Analog Modulation :** Introduction, Receiver Model, Noise in DSB-SC receivers, Noise in AM receivers, Threshold effect, Noise in FM receivers, Capture effect, FM threshold effect, FM threshold reduction, Pre-emphasis and De-emphasis in FM (refer Chapter 6 of Text). **Sampling And Quantization:** Introduction, Why Digitize Analog Sources?, The Low pass Sampling process Pulse Amplitude Modulation.	07	L1, L2, L3.
5	**Sampling And Quantization:** Time Division Multiplexing, Pulse-Position Modulation, Generation of PPM Waves, Detection of PPM Waves. The Quantization Random Process, Quantization Noise, Pulse–Code Modulation: Sampling, Quantization, Encoding, Regeneration, Decoding, Filtering, Multiplexing (refer Chapter 7 of Text)	08	L1, L2, L3.

Note 1: Each Unit will have Internal Choice

Note 2: Two assignments are evaluated for 5 marks: Assignment - 1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes: After the completion of the Course the student should be able to :

CO1 Associate and apply the concepts of Low pass sampling, reconstruction to Digital transmitters and receivers used in cellular and other communication devices.

CO2 Analyze and compute performance of FM modulation and digital formatting.

CO3 Test and validate digital formatting schemes with quantization noise under noisy channel conditions to estimate the performance in practical communication systems.

CO4 Design/Demonstrate by way of simulation or emulation the functional blocks of digital formatting.

CO5 Demonstrate their ability to use appropriate engineering mathematical concepts in qualitatively problems pertaining to the Rectifiers, Regulators, Amplifiers, Op-Amp.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO3,PO5,PO6

CO2 PO1,PO2,PO5,PO5,PO6

CO3 PO1,PO2,PO3,PO5,PO6

CO4 PO1,PO2,PO3,PO5,PO6

CO5 PO1,PO2,PO5,PO5,PO6

Text Books.

1 **"Communication Systems"**, Simon Haykins & Moher, 5th Edition, John Willey, India Pvt. Ltd, 2010, ISBN 978 – 81 – 265 – 2151 – 7.

Reference Text Books.

1 **Modern Digital and Analog Communication Systems**, B. P. Lathi, Oxford University Press., 4th edition.

2 **An Introduction to Analog and Digital Communication**, Simon Haykins, John Wiley India Pvt. Ltd., 2008, ISBN 978–81–265–3653–5.

3 **Principles of Communication Systems**, H.Taub & D.L.Schilling, TMH, 2011.

4 **Communication Systems**, Harold P.E, Stern Samy and A.Mahmond, Pearson Edition, 2004.

Web Links.

1 www.nptel.in

Active learning Assignments (AL) : Preparation of power-point slides, which include videos, animations, pictures, graphics for better understanding theory and practical work – The faculty will allocate chapters/ parts of chapters to groups of students so that the entire syllabus to be covered. The power-point slides should be put up on the web-site of the College/ Institute, along with the names of the students of the group, the name of the faculty, Department and College on the first slide. The best three works should submit to ECE Department, Dr. AIT.

Sub Title : Verilog HDL		
Sub Code:18EC44	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Assignment + SEE = 45 + 05 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Describing the EDA flow of digital design and recognizing the importance of HDL.
2. Able to design and analyze the digital circuits using dataflow and gate level modeling.
3. Implementation of digital circuits at behavioral level.
4. Understand the concepts of tasks and functions.
5. To gain the knowledge on synthesis of digital design and understanding the various logic devices available for the synthesis.

UNIT No	Syllabus Content	Bloom's Taxonomy	Hrs
1	**Overview of digital design with Verilog HDL:** Evolution of Computer Aided Digital Design, Emergence of HDLs, Typical Design flow, Importance of HDLs, Popularity of Verilog HDL, Trends in HDLs. **Hierarchical Modeling Concepts:** Design Methodologies, Modules, Instances, Components of a Simulation, Example **Text-1**		08
2	**Basic Concepts:** Lexical Conventions, Datatypes, System tasks and Compiler directives **Modules and ports:** Modules, Ports, Hierarchical Names.		08
3	**Gate Level Modeling:** Gate types, Gate delays. **Data Flow Modeling**: Continuous assignments, Delays, Expressions, Operators, and operands, operator types, Examples. **Text-1**		08
4	**Behavioral Modeling:** Structured Procedures, Procedural Assignments, Timing controls, Conditional statements, Multiway branching, Loops, Sequential and Parallel Blocks, Generate blocks, Examples. **Modeling Examples:** Register, State Machine Modeling, Interacting State Machines, Modeling a Moore FSM, Modeling a Mealy FSM. **Text-1 & Text-2**		08
5	**Tasks and functions:** Difference between Tasks and Functions, Tasks, Functions. **Useful Modeling Techniques:** Procedural Continuous Assignments, Overriding Parameters, Conditional compilation and Execution, Time scales **Text-1**		07

Note 1. Each unit will have internal choice

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2. Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1. Understand the HDL design flow and lexical conventions of the language.
CO2. Ability to design combinational and sequential circuits in different styles.
CO3. Able to design and test the circuits using behavioral modeling.
CO4. Ability to design the circuits using the subroutines and to model FSM in Verilog.
CO5. Ability to understand the concept of synthesis and programmable logic device.

Cos	Mapping with POs
CO1	PO2,PO3
CO2	PO2,PO3
CO3	PO2,PO3
CO4	PO2,PO3
CO5	PO2,PO3,PO4

TEXT BOOKS:

1. Samir Palnitkar, **"Verilog HDL – A guide to Digital Design and Synthesis",** Pearson, 2003.
2. J. Bhasker," **A verilog HDL Primer**" BS Publications , 2nd Edition.
3. Stephen Brown, ZvonkoVransic," **Fundamentals of digital logic with verilog Design**", TMH,2 nd Edition.

REFERENCE BOOKS/WEB LINKS:

1. Charles H. Roth, "**Digital Systems Design Using VHDL**", Thomson Learning, Inc, 1st Edition, 2002.
2. D Perry, "**Introduction to VHDL programming**", 4th Edition ,2002
3. Floyd, " **Digital Fundamentals using VHDL**", Pearson Education, 2nd Edition, 2003

Subject Title : Signals and System

Sub.Code: 18EC45 | No. of Credits:04=4:0:0 (L - T – P) | No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs | CIE+Assignment +SEE=45+5+50=100 | Total No.of Contact Hours:52

Course Learning Objectives: The student should be able to:

1 Understand the mathematical description of continuous and discrete time si systems.
2 Analyze the signals in time domain using convolution difference/differential equations
3 Classify signals into different categories based on their properties.
4 Analyze Linear Time Invariant (LTI) systems in time and transform domains.

Unit No	Syllabus Contents	No. of Hours	
1	**Introduction and Classification of signals:** Definition of signal and systems, communication and control systems as examples. (Text1:1.1,1.2) **Classification of signals. Basic Operations on signals:** Amplitude scaling, addition, multiplication, differentiation, integration, time scaling, time shift and time reversal. (Text1:1.4,1.5) **Elementary signals/Functions:** Exponential, sinusoidal, step, impulse and ramp functions. Expression of triangular, rectangular and other waveforms interms of elementary signals. (Text1:1.6)	09	L1,L2,L3
2	**System Classification and properties:** Linear-nonlinear, Time variant-invariant, causal-noncausal, static-dynamic, stable-unstable, invertible.(Text1:1.8) **Time domain representation of LTI System:** Impulse response, convolution sum, convolution integral. Computation of convolution sum and convolution integral using graphical method for unit	12	L1,L2, L3

Unit No	Syllabus Contents	No. of Hours	
	step and unit step, unit step and exponential, exponential and exponential, unit step and rectangular, and rectangular and rectangular(Text1:2.1,2.2)		
3	**LTI system Properties interms of impulse response:** System interconnection, Memoryless, Causal, Stable, Invertible and Deconvolution, and step response. (Text1:2.3) **Differential & Difference Equation representation of LTI systems:** Solution for Differential & Difference equations. (Text1:2.4)	09	L1,L2, L3,L4
4	**Fourier Representation of periodic and aperiodic Signals:** Introduction to CTFS, Introduction to Fourier Transform & DTFT, Definition and basic problems. (Text1:3.1,3.2,3.15.1) **Properties of Fourier Transform**: Linearity, Symmetry, Time shift, Frequency shift, Scaling, Differentiation and Integration, Convolution and Modulation, Parsevals relationships and Duality. (Text1:3.11)	09	L1,L2, L3,L4
5	**The Z-Transforms :** Z transforms, properties of the region of convergence, Inverse Z-transform, Causality and stability, Transform analysis of LTI systems, The unilateral Z-transform. (Text1:7.1,7.2,7.3,7.5,7.6,7.8)	13	L1,L2, L3,L4

Note 1: Each Unit will have Internal Choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5

Course Outcomes: After the completion of the Course the student should be able to :

CO1 Analyze the different types of signals and systems.

CO2 Determine the linearity, causality, time-invariance and stability properties of continuous and discrete time systems

CO3 Represent continuous and discrete systems in time and frequency domain using different transforms

CO4 Test whether the system is stable.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO3

CO2 PO1,PO2,PO3,PO4

CO3 PO1,PO2,PO3,PO4

CO4 PO1,PO2,PO3,PO4

Text Books.

1 Simon Haykin and Barry Van Veen, "Signals and Systems", Edition, John Wiley & Sons, 2001, 2010.

2 Ganesh Rao and Satish Tunga, "Signals and Systems", Pearson/Sanguine

Reference Text Books.

1 Michael Roberts, "Fundamentals of Signals & Systems", 2nd edition, Tata McGraw-Hill, 2010, ISBN 978-0-07-070221-9.

2 Alan V Oppenheim, Alan S, Willsky and A Hamid Nawab, "Signals and Systems" Pearson Education Asia / PHI, 2nd edition, 1997. Indian Reprint 2002.

3 H. P Hsu, R. Ranjan, "Signals and Systems", Scham's outlines, TMH, 2006.

4 V. Krishnaveni and A. Rajeswari, "Signals and Systems", Wiley India, Reprint , 2012

5 B. P. Lathi, "Linear Systems and Signals", Oxford University Press, 2005.

6 Uday Kumar S"Signals and System",5th Edition,Prism Books Pvt.Ltd.,2009-10

Web Links.

1 www.nptel.in

2 https://www.youtube.com/watch?v=w8Dq8blTmSA

Active learning Assignments (AL) : Preparation of power-point slides, which include videos, animations, pictures, graphics for better understanding theory and practical work – The faculty will allocate chapters/ parts of chapters to groups of students so that the entire syllabus to be covered. The power-point slides should be put up on the web-site of the College/ Institute, along with the names of the students of the group, the name of the faculty, Department and College on the first slide. The best three works should submit to ECE Department, Dr. AIT.

Subject Title : Computer Organization and Architecture

Sub.Code: 18EC46 | No. of Credits:03=2:2:0 (L - T – P) | No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs. | CIE+Assignment +SEE=45+5+50=100 | Total No.of Contact Hours:39

Course Learning Objectives: The student should be able to:

1. Understand the meaning of basic structure of computers, and machine instructions and programs.
2. Analyze addressing modes and assembly language.

3. Compute the quantitative parameters for functions of input and output organization.
4. Associate the concepts of memory system

Unit No	Syllabus Contents	No. of Hours	Blooms Taxnomy level.
1	**Basic Structure of Computers:** Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance – Processor Clock, Basic Performance Equation (upto 1.6.2 of Chap 1 of Text). **Machine Instructions and Programs**: Numbers, Arithmetic Operations and Characters, IEEE standard for Floating point Numbers, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing, (upto 2.4.6 of Chap 2 and 6.7.1 of Chap 6 of Text).	8	L1,L2,L3
2	Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions (from 2.4.7 of Chap 2, except 2.9.3, 2.11 & 2.12 of text).	8	L1,L2,L3
3	**Input/Output Organization:** Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Direct Memory Access, (upto 4.2.4 and 4.4 except 4.4.1 of Chap 4 of text).	8	L1,L2,L3
4	**Memory System:** Basic Concepts, Semiconductor RAM Memories-Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories, Virtual Memories, Secondary Storage-Magnetic Hard Disks (5.1, 5.2,	8	L1,L2,L3

Unit No	Syllabus Contents	No. of Hours	Blooms Taxnomy level.
	5.2.1, 5.2.2, 5.2.3, 5.3, 5.5 (except 5.5.1 to 5.5.4), 5.7 (except 5.7.1), 5.9, 5.9.1 of Chap 5 of Text).		
5	**Basic Processing Unit:** Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Microprogrammed Control (upto 7.5 except 7.5.1 to 7.5.6 of Chap 7 of Text).	7	L1,L2,L3

Note1: Each Unit will have Internal Choice

Course Outcomes: After the completion of the course the student should be able to:

CO1 Associate the concepts of structure of computer.

CO2 Analyse and model the machine instruction and programs.

CO3 Analyse and addressing modes.

CO4 Demonstrate the input/output organization

CO5 Demonstrate the memory system.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO3,PO5

CO2 PO1,PO2,PO5

CO3 PO1,PO2,PO3

CO4 PO1,PO2,PO3

CO5 PO1,PO2,PO5

Text Books.

1 Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition, Tata McGraw Hill, 2002.

Reference Text Books.

1 David A. Patterson, John L. Hennessy: Computer Organization and Design – The Hardware / Software Interface ARM Edition, 4th Edition, Elsevier, 2009.
2 William Stallings: Computer Organization & Architecture, 7th Edition, PHI, 2006.
3 Vincent P. Heuring & Harry F. Jordan: Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.

Subject Title : Analog Circuits and Communication Laboratory

Sub.Code: 18EC47	No. of Credits:02	No. of Lecture Hours/Week : 04
Exam Duration:03 Hrs	02Hr Tutorial (Instructions) + 02 Hours Laboratory	Total No.of Contact Hours:

Course Learning Objectives: The student should be able to:

1 Understand the circuit configurations and connectivity of BJT and FET Ampl Study of frequency response.
2 Design and test of analog circuits using OPAMPs
3 Design and test the communication circuits for different analog modulation schemes.
4 Understand the sampling and reconstruction using simple circuits

Unit No	Syllabus Contents	Blooms Levels	L1, L2, L3
1	Design and setup the Common Source JFET/MOSFET amplifier and plot the frequency response.		
2	Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain- bandwidth product from its frequency response.		
3	Design and set-up i) Colpits Oscillator ii)Hartley Oscillator and iii)Crystal Oscillator		
4	Design active second order Butterworth low pass and high pass filters.		
5	Design Adder, Integrator and Differentiator circuits using Op-Amp		
6	Test a comparator circuit and design a Schmitt trigger for the given UTP and LTP values and obtain the hysteresis.		
7	Design 4 bit R – 2R Op-Amp Digital to Analog Converter (i) using 4 bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.		
8	Design a circuit using LM741 and LF398 to generate Amplitude modulation and DSBSC signal.		
9	Design of Monostable and Astable Multivibrator using 555 Timer.		
10	Frequency modulation using IC 8038/2206 and demodulation		
11	BJT/FET Mixer		

Unit No	Syllabus Contents	Blooms Levels	L1, L2, L3
12	Pulse sampling, flat top sampling and reconstruction		

Course Outcomes: After the completion of the Course the student should be able to :

CO1 Design of analog circuits using BJTs and FETs and evaluate their performance characteristics.

CO2 Design of analog circuits using OPAMPs for different applications

CO3 Understand the use of transistor in the design of continuous or pulse modulation schemes.

CO4 Understand the use of ICs in circuit designs for AM and FM modulation and demodulation

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1,PO2,PO3,PO5

CO2 PO1,PO2,PO5

CO3 PO1,PO2,PO3

CO4 PO1,PO2,PO3

CO5 PO1,PO2,PO5

Text Books.

1 K. A. Navas, "Electronics Lab Manual", 5th edition, PHI, 2015.

Sub Title : HDL LAB		
Sub Code:18ECL48	**No of Credits : 2:0:2:2(L:T:P)**	**No of lecture hours/week : 03 2Hr :Tutorial +2Hr: Laboratory**
Exam Duration : 03 Hours	**CIE +Assignment + SEE = 50 + 50 =100**	**RBT Level : L1,L2,L3**

Course objectives:

1. Acquire skills to develop programs to design digital circuits in various modeling styles.
2. Verify the designs by simulation tools such as Altera/Xilinx.
3. To synthesize the designs on FPGA/CPLDs.
4. Interface hardware to programmable ICs through I/O ports.

Unit No.	Syllabus contents	No of Hours
	PART-A	
1	Write the Verilog to simulate and synthesize the all gates and binary to gray converter.	3
2	Write the Verilog code with test bench to simulate and synthesize the following 2 to 4 decoder and encoder (with & without priority)	3
3	Write the Verilog code and its test bench to simulate and synthesize 1-bit full adder, 3-bit carry look ahead adder and 4-bit ripple carry adder.	3
4	Write the hardware description code and test bench for 4-bit ALU. An ALU is a hardware that can give the result of various arithmetic and logical operations of the two numbers based on a control signal.	3
5	Write the Verilog code to simulate and synthesize the digital circuits by using generate blocks.	3
6	Simulate and synthesize the SR, D, JK and T flip-flops.	3
7	Design and develop the Verilog code for 4-bit synchronous binary up/down counter, 4-bit asynchronous binary up/down counter, any sequence counter and Ring counter.	3
8	Write a program to illustrate the function and tasks.	3
	PART-B Interfacing Programs	
9	Write the Verilog code to control external light using relay.	3
10	Write Verilog code to generate different waveforms (Sine, Square, Triangle and Ramp) vary the frequency and amplitude using DAC.	3
11	Write HDL code to control speed and direction of DC motor and stepper motor.	3
12	Write HDL code to display messages on an alpha numeric LCD display.	3

Course Outcomes:

CO1. Design, Simulation and synthesis of various digital circuits.
CO2. Waveforms generation using FPGA.
CO3. Synthesize Combinational and Sequential circuits on programmable ICs and test the hardware.
CO4. Interface the hardware to the programmable chips and obtain the required output.

Cos	Mapping with POs
CO1	PO2,PO3
CO2	PO2,PO3

CO3	PO2,PO3
CO4	PO2,PO3
CO5	PO2,PO3,PO4

TEXT BOOKS:

1. Samir Palnitkar, **"Verilog HDL – A guide to Digital Design and Synthesis",** Pearson, 2003.
2. J. Bhasker," **A verilog HDL Primer**" BS Publications , 2nd Edition.
3. Stephen Brown, ZvonkoVransic," **Fundamentals of digital logic with verilog Design**", TMH,2 nd Edition.

REFERENCE BOOKS/WEB LINKS:

1. Charles H. Roth, "**Digital Systems Design Using VHDL**", Thomson Learning, Inc, 1st Edition, 2002.
2. D Perry, "**Introduction to VHDL programming**", 4th Edition ,2002
3. Floyd, " **Digital Fundamentals using VHDL**", Pearson Education, 2nd Edition, 2003

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2018 Batch)

V Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	PC	18HS51	IPR	HS	03	--	--	03	050	050	100	03
2	PC	18EC51	Electromagnetic Waves	EC	04	--	--	04	050	050	100	03
3	PC	18EC52	Digital Signal Processing	EC	04	--	--	04	050	050	100	04
4	PC	18EC53	Digital Communication	EC	04	--	--	04	050	050	100	04
5	PC	18EC54	Microprocessor and Microcontroller	EC	03	--	--	04	050	050	100	03
6	PE	18EC55X	Professional Elective-1	EC	03	--	--	03	050	050	100	03
7	OE	18ECEXX	Open-Elective A		03	--	--	03	050	050	100	03
8	PC	18ECL56	Microcontroller Laboratory	EC	--	--	02	02	050	050	100	01
9	PC	18ECL57	Digital Signal Processing Laboratory	EC	--	--	02	02	050	050	900	01
				Total	**24**	**00**	**04**	**29**	**400**	**450**	**800**	**25**

18EC55x_Professional Elective – 1		
Sl. No.	**Course Code**	**Course Title**
1	18EC551	Digital Switching System
2	18EC552	Programming with Python
3	18EC553	Artificial Neural Networks
4	18EC554	Object Oriented Programming with C++
5	18EC555	Control Systems

Open Elective-A(OE-A)		
Sl. No.	**Course Code**	**Course Title**
1	18ECE01	Real Time Operating System(CS,IS, EI, ML)
2	18ECE02	Mechatronics (CS,IS, EI, ML, ME, IEM, EEE)
3	18ECE03	Television Engineering (TE, EI, ML)
4	18ECE04	Sensors (CS, IS, ML, TC)

BOS Chairman Dean(Academics) Principal

Sub Title : Electromagnetic Waves		
Sub Code: 18EC51	**No. of Credits:3=2 : 1 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. Understanding the concepts of vectors, electric fields for EM waves and to analyze and solve problems using coulomb's law, gauss law.
2. Understanding the concepts of energy density, potential difference and capacitance.
3. Understanding the Biot Savart law, Laplace and Poisson's equations and to acquire knowledge of their practical applications.
4. Understanding the importance of Maxwell's equation and applying them for time varying fields.
5. To understand the importance of wave propagation in free space & dielectrics and applying them for time varying fields.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Electrostatics:** Coulomb's Law and electric field intensity, Field due to continuous volume charge distribution, Field of a line charge. Field of a sheet of charge. Electric flux density, Gauss' law and its applications. Divergence, Maxwell's First equation (Electrostatics), vector operator ∇ and divergence theorem **TEXT 1**	11	L1, L2, L3.
2	**Energy and potential:** Energy expended in moving a point charge in an electric field, The line integral, Definition of potential difference and Potential, The potential field of a point charge and system of charges, Potential gradient , Energy density in an electrostatic field. **C**apacitance and examples. **TEXT 1**	09	L1, L2,L3
3	**Poisson's and Laplace's equations:** Derivations of Poisson's and Laplace's Equations, Uniqueness theorem, Examples of the solutions of Laplace's and Poisson's equations. **Steady magnetic field:** Biot-Savart law and its applications, Ampere's circuital law and its applications, magnetic flux and flux density, scalar and Vector magnetic potentials. **TEXT 1**	11	L1,L2,L3,L4
4	**Magnetic forces** - Force on a moving charge and differential current element, Force between differential current elements. **Maxwell's equations:** Inductance and examples, Faraday's law, Displacement current. Maxwell's equation in point and Integral form, Boundary conditions for perfect dielectric materials, magnetic boundary conditions. **TEXT 1**	11	L1,L2,L3,L4
5	**Electromagnetic waves:** Wave propagation in free space and dielectrics, Poynting's theorem. Propagation in good conductors – skin effect. Wave polarization. Reflection of uniform plane waves at normal incidence, standing wave ratio. **TEXT 1**	10	L1,L2,L3,L4

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3. Unit 1- Digital Teaching and Learning

Course Outcomes: After the completion of the Course the student are:

CO1. Able to define electrostatic and magnetic field laws such as Coulomb's law, Gauss' law, potential gradient, Biot-Savart law, Maxwell's equations and Wave polarization.

CO2. Able to understand wave propagation, electric and magnetic fields in different system of charges and also able to explain Maxwell's equations and potential Energy.

CO3. Able to apply and solve Divergence, Potential gradient in electrostatic fields & Ampere's circuital law, Curls in magnatostatic fields and also able to solve and apply Maxwell's equations in wave propagation.

CO4. Able to analyse Poisson's, Laplace & Maxwell's equations and propagation of waves in different medium with its fundamental concepts.

Cos	Mapping with POs	Mapping with PSOs
CO1	PO1,PO2,PO8,PO9,PO10,PO12	PSO1,PSO2,PS03
CO2	PO1,PO2,PO3,PO4,PO8,PO9,PO10,PO12	PSO1,PSO2,PS03
CO3	PO1,PO2,PO4,PO5,PO7,PO8,PO9,PO10,PO11,PO12	PSO1,PSO2, PS03
CO4	PO1,PO2,PO4,PO5,PO6,PO7,PO8,PO9,PO10,PO11,PO12	PSO1,PSO2, PS03

Text Book:	
1.	William H Hayt Jr. and John A Buck, "**Engineering Electromagnetics**", 8th edition, McGraw-Hill, **2012**
2.	David K Cheng, "**Field and Wave Electromagnetics**", 2nd edition, Pearson Education Asia, Indian Reprint – 2001

Reference Books:	
1.	John Krauss and Daniel A Fleisch , "**Electromagnetics with Applications**", 5th edition, McGraw-Hill, **1999**
2.	Edward C. Jordan and Keith G Balmain,, "**Electromagnetic Waves and Radiating Systems**", 2nd Edition, Prentice – Hall of India / Pearson Education, Reprint – ***2002***

Web Links:	
1.	www.nptel.in
2.	www.google.com , david k cheng fields and waves electromagnetics pdf download
3.	www.google.com, william h hayt engineering electromagnetics pdf
4.	www.youtube/electromagnaticsforengineers

Sub Title : Digital Signal Processing		
Sub Code: 18EC52	**No. of Credits:3=2 : 2 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : 3 Hours	**CIE + Group Activity + Assignment + SEE =40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. To learn and understand sampling process, invertible systems, Discrete Fourier Transforms, Fast Fourier Transforms, IIR filters , FIR filters and their structures
2. To interpret the sampling process, Inverse Systems, DFT and their properties, FFT algorithms, IIR and FIR filters
3. To apply the concept of sampling theorem, DFT, FFT algorithms, IIR and FIR filters
4. To illustrate the DFT, FFT algorithms, IIR and FIR filters
5. To design the analog IIR, digital IIR and FIR filters

UNIT No	Syllabus Contents	No of Hours
1	**Sampling and Invertible systems:** Analog to digital conversion, Sampling of analog signals, Sampling theorem. Inverse systems and de-convolution, Invertibility of LTI systems, minimum phase, maximum phase and mixed phase systems. **TEXT 1 and TEXT 2**	10
2	**Discrete Fourier Transform (DFT) and its Properties:** Frequency domain sampling and reconstruction of discrete time signals: DFT and IDFT, Numerical examples. Properties of DFT: Periodicity, linearity, Symmetry properties, Circular folding, Circular Convolution, Circular time shift, Circular frequency shift, Complex conjugate property, Multiplication of two sequences, Use of DFT in linear filtering, overlap-save and overlap-add method. **TEXT 1 and TEXT 2**	10
3	**Fast-Fourier-Transform (FFT) Algorithms:** Direct computation of DFT, need for efficient computation of the DFT (FFT algorithms). Radix-2 FFT algorithm for the computation of DFT and IDFT: Decimation-in-time (DIT) and Decimation-in-frequency (DIF) algorithms. **TEXT 1**	11
4	**IIR Filter Design:** Characteristics of commonly used analog filters – Butterworth and Chebyshev filters, analog to analog frequency transformation. **Design of IIR Digital filters from analog filters (Butterworth and Chebyshev Type):** Impulse Invariance method and Bilinear transformation method, Derivation and design problems. **TEXT 1**	10
5	**FIR Filter Design:** Introduction to FIR filters, Design of FIR filters using Rectangular, Hamming and Hanning windows. **Implementation of Discrete-Time Systems:** Structures for IIR systems: Direct form I & II, Cascade & Parallel form realization. Structures for FIR systems: Direct form, Linear phase, Cascade form. **TEXT 1 and TEXT 2**	11

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2

Assignment - 2 from units 3, 4 and 5

Note 3.Unit 3 will be taught by online and digital platform

Course Outcomes:

CO1 Define the sampling process, invertible systems, Discrete Fourier Transforms, Fast Fourier Transforms, IIR and FIR filters and their structures

CO2 Understand sampling process, Inverse Systems, DFT and their properties, FFT algorithms and IIR and FIR filters.

CO3 Analyze DFT, FFT algorithms, IIR and FIR filters.

CO4 Apply the concept of sampling theorem, DFT, FFT algorithms, IIR and FIR filters.

CO5 Design the analog IIR, digital IIR and FIR filters.

Cos	Mapping with POs
CO1	PO1,PO8
CO2	PO2,PO6,PO7
CO3	PO4,PO7,PO8
CO4	PO5,PO6,PO8
CO5	PO3,PO10,PO12

Text Book:	
1.	**Proakis & Monalakis,** "Digital Signal Processing-Principles, Algorithms & Applications", Fourth Edition, Pearson Education, New Delhi, 2009
2.	**Emmanuel C Ifeachor and Barrie W Jervis,** "Digital Signal Processing: A Practical Approach", Second edition, Pearson Education, New Delhi, 2002

Reference Books:	
1.	**Alan V. Oppenheim and Schaffer**, "Discrete Time Signal Processing", 2nd edition, PHI, 2007
2.	**Sanjit K. Mitra,** "Digital Signal Processing", 3rd edition, Tata Mc-Graw Hill, 2010
3.	**Lee Tan**, "Digital Signal Processing", edition, Elsevier publications, 2007
4.	**Shenoy**, "Introduction to Digital Signal Processing and Filter Design", 1st edition, John Wiley & Sons, 2010
5.	**Lonnie C. Ludeman,** "Fundamentals of Digital Signal Processing", International edition, John Wiley & Sons, 1988

Web Links.

1 http://nptel.ac.in/courses/117102060/

2 https://ocw.mit.edu/resources/res-6-008-digital-signal-processing-spring-2011/study-materials/

Sub Title : DIGITAL COMMUNICATION		
Sub Code: 18EC53	**No. of Credits: 4 = 4 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration: 3 Hours	**CIE +Assignment + SEE = 45 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. A brief overview of the digital communication system and the techniques of formatting the source signal.
2. Demonstrate key concepts like geometrical analysis of signals, probability of error, various receiver types in detection.
3. Understand and analyze different waveform coding techniques and applications and spread spectrum modulation.
4. Understand information on discrete PAM signals, ISI and adaptive equalization for data transmission.
5. Analyze and design of digital modulation techniques and performance analysis based on probability of error.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	Introduction: Sources and signals, Basic signal processing operations in digital communications, Channels for digital communication. Detection and Estimation: Model of Digital communication system, Gram-Schmidt Orthogonalization Procedure, geometric interpretation of signals, response of bank of correlators to noisy input, Detection of known signals in noise, probability of error, correlation receiver, matched filter receiver. Text 1, Text 2 and Text 3	13	L1, L2, L3.L4
2	Sampling Process: Sampling Theorem, signal space interpretation, Quadrature sampling of Band pass signal, PAM, TDM. Waveform Coding Techniques: Pulse Code Modulation, channel noise and error probability, Quantization noise and Signal to Noise Ratio, robust quantization, DPCM, DM Text 1 & Text 2	12	L3,L4,L5
3	Base-Band Shaping for Data Transmission: Discrete PAM signals, power spectra of discrete PAM signals, Inter Symbol Interference, Nyquist's criterion for distortion less base-band binary transmission, correlative coding, eye pattern. Text 1 &Text 2	09	L3,L4
4	Digital Modulation Techniques: Digital Modulation formats. Coherent binary modulation techniques: Binary ASK, PSK, and FSK. Coherent Quadrature modulation techniques: Quadriphase-shift keying (QPSK). Non-coherent binary modulation techniques: Differential phase shift keying (DPSK). Text 1 &Text 2	09	L2,L3, L4,L5

5	Spread Spectrum Modulation: Pseudo noise sequences, notion of spread spectrum, Principle of Direct Sequence Spread Spectrum (DSSS), frequency hop spread spectrum. Multiplexing and Multiple Access: FDMA, TDMA, CDMA and SDMA Text 1 & Text 3	09	L1,L2,L3

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.
Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1. Able to understand the System approach to Digital communication right at the foundation level and various basic signal processing operations involved.

CO2. Gain the knowledge on the key concepts such as signal space concepts, probability of error, and analyse the detection of signals using correlation receiver and matched filter.

CO3. Gain the knowledge on the sampling process, waveform coding techniques and quantization techniques to improve performance of the digital communication system.

CO4. Capable of analysing Discrete PAM signals and its power spectra and knowledge on to ISI and measures to counter ISI problem using raised cosine filter and correlative coding methods.

CO5. Able to describe the spread spectrum type of communication along with its advantages and know briefly the various multiple access techniques compare them.

Cos	**Mapping with POs**	**Mapping with PSOs**
CO1	PO1,PO2,PO4,PO6	PSO1,PSO2,PS03
CO2	PO1,PO2, PO6	PSO1,PSO2,PS03
CO3	PO1,PO2,PO4,PO6	PSO1,PSO2, PS03
CO4	PO1,PO2PO3,PO4,PO5,PO6	PSO1,PSO2, PS03
CO5	PO1,PO2PO3,PO4,PO5,PO6	PSO1,PSO2,PS03

Text Book:	
1.	Simon Haykins, “Digital Communications”, 4th Edition, John Wiley, 2008(reprint).
2.	Dr. K. N. Hari Bhat & Dr. D. Ganesh Rao, ”Digital communications”, 2nd Edition, Sanguine technical publications, 2008. (Reprint).
3.	Bernard Sklar,” Digital communications”, 3rd Edition, Pearson education, 2007

Reference Books:	
1.	K.Sam Shanmugam, “Digital and analog communication systems”,4th Edition, John Wiley, 1996.
2.	John Proakis, Masoud Salehi,” Digital communications”, 5th Edition, Mac Graw Hill, 2008.
3.	Barry, John R., Lee, Edward A., Messerschmitt, David G,” Digital communications”, 3rd Edition, Springer, 2004
4.	B. P. Lathi, Zhi Ding, “Modern Digital and Analog Communication Systems”, 4th Edition, Oxford, 2009.

Web Links:	
1.	1 http://nptel.ac.in/ online course /Digital Communication
2.	https://lecturenotes.in/subject/45/digital-communication-techniques-dct
3.	https://mrcet.com/downloads/digital_notes/ECE/III%20Year/DIGITAL%20COMMUNICATIONS.pdf

Sub Title : Microprocessor and Microcontrollers		
Sub Code: 18EC54	**No. of Credits:3= 2 : 1 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. To learn the architecture of 8086 microprocessor, 8051 microcontroller and MSP 430
2. To learn the memory organization of MCS51 and MSP 430. I/O ports and memory interfacing techniques with MCS51.
3. To learn the Instruction set of MCS51 and able to write the assembly language programs and c programs.
4. To learn the Timer/Counter, serial port configurations and able to write programs.
5. To learn the interrupts of MCS51 and MSP 430 able to Interface peripherals with MCS51.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction to microprocessors and microcontrollers:** RISC & CISC CPU Architectures, Harvard & Von- Neumann CPU architecture. **The 8086 Processors:** 8086 Architecture, CPU Architecture-BIU and EU, Register organization, Memory organization and segmentation, pin functions of 8086**.(TEXT 1 and TEXT 2)**	10	L1, L2, L3
2	**8051 Microcontroller:** The 8051 Architecture, Pin diagram of 8051, Memory organization, External Memory interfacing. Classification of Instruction, Addressing modes: Immediate addressing, Register addressing, Direct addressing, Indirect addressing, relative addressing, Absolute addressing, bit direct addressing. **8051 Instructions :** 8051 instructions, Data transfer instructions**.(TEXT 2)**	09	L1,L2,L3
3	**8051 Instructions and Programming:** Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instruction. 8051 programming: Assembler directives, Assembly language programs and Time delay calculations. Stack operations. Introduction to Embedded C, C data types, logical operations, programming 8051 using embedded C**.(TEXT 2 and TEXT 3**)	11	L1,L2,L3,L4
4	**Timers/counters:** 8051 timers/counters, programming 8051 timers in assembly and C. Data communication, Basics of Serial Data Communication, 8051 Serial Communication, Programming in assembly and C. **8051 interrupts and interfacing:** Interrupts and Basics of interrupts, 8051 Interfacing and Applications: Basics of I/O concepts, I/O Port Operation, Interfacing 8051 to DAC, interfacing of Keyboard. **(TEXT 3)**	12	L1,L2,L3,L4,L6
5	**MSP430 Architecture:** Introduction – Where does the MSP430 fit, The outside view, The inside view-Functional block diagram, Memory, Central Processing Unit, Memory Mapped Input and Output, Clock Generator, Exceptions: Interrupts and Resets, MSP430 family**.(TEXT 4)**	10	L1,L2,L3,L4,L6

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.
Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.
Note 3. Unit 5 taught through Digital Learning.

Course Outcomes:

CO1. Understand the architecture and features of 8086 microprocessor, 8051 microcontrollers and MSP 430.
CO2. Understand the memory organization and memory mapping of MCS51 and MSP 430.
CO3. Understand the instruction sets of MCS51 and able to write Assembly and High-level Programs.
CO4. Explain the TIMER/COUNTER configuration able to implement by programs to generate time delay/counting.
CO5. Explain the Interrupt and serial communication and able to apply for real time applications.

Cos	Mapping with POs
CO1	PO1, PO5,PO6,PO7,PO8,PO12
CO2	PO1, PO2, PO3, PO5,PO6,PO8,PO9,PO12
CO3	PO1, PO2, PO3, PO5,PO6,PO8,PO9,PO12
CO4	PO1, PO2, PO3, PO5,PO6,PO8,PO9,PO12
CO5	PO1,PO2, PO3, PO5,PO6,PO7,PO8,PO11, PO12

Text Book:

1. **Yu-cheng Liu, Glenn A.Gibson,** "Microcomputer Systems: The 8086/8088 Family Architecture, Programming, and Design"
2. **Kenneth J. Ayala,** "The 8051 Microcontroller Architecture, Programming & Applications", 2e Penram International, 1996 / Thomson Learning 2005.
3. **Muhammad Ali Mazidi, Janice Gillespie Mazidi and Rollin D. McKinlay,** "The 8051 Microcontroller and Embedded Systems – using assembly and C", PHI, 2006 / Pearson, 2006.
4. **John Davies,** "MSP430 Microcontroller Basics", Elsevier, 2010.

Reference Books:

1. **Doughlas V. Hall**, "Microprocessors and Interfacing Programming and Hardware".

Web Links:

1. "MCS51 Microcontroller family user's manual"
   "MSP430 Web material", Texas Instruments, 2008.
2. https://swayam.gov.in/nd1_noc20_cs25

Sub Title : DIGITAL SWITCHING SYSTEM

Sub Title: Digital Switching System		
Sub Code: 18EC551	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Analyze basic switching techniques used in telephone system.
2. Analyze the different types of calls in DSS
3. Analyze time division and space division switching techniques and integrate both to improve Performance the course learning objective
4. Analyze different signaling techniques associated with telephone network.
5. Analyze switching networks with various techniques

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**DEVELOPMENTS OF TELECOMMUNICATIONS**: Network structure, Network services, terminology, Regulation, Standards, telecommunications transmission, Power levels, Four wire circuits, Digital transmission, FDM, TDM . **EVOLUTION OF SWITCHING SYSTEMS:** Message switching, Circuit switching, Functions of switching systems, distributed frames, crossbar systems Electronic switching. (TEXT 1 and TEXT 2)	8	L1,L2,L3.
2	**TELECOMMUNICATION TRAFFIC:** Unit of traffic, Congestion, Traffic measurement, Mathematical model, lost call systems, Queuing systems. **SWITCHING SYSTEMS FUNDAMENTALS** : Introduction Purpose of analysis, Basic central office linkages, Outside plant versus inside plant, Switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems DSS fundamentals Building blocks of a digital switching system, (TEXT 1 and TEXT 2)	8	L1,L2,L3.
3	**COMMUNICATION AND CONTROL:** Introduction scope Switching communication and control Basic functions of interface controller Basic functions of network control processor Basic functions of central processor call processing. **SWITCHING SYSTEM SOFTWARE**: Introduction, Scope, Basic software architecture, Call models, Software linkages during call. (TEXT 1 and TEXT 2)	8	L1,L2,L3.
4	**A GENERIC DIGITAL SWITCHING SYSTEM MODEL:** Introduction, Scope, Hardware and Software architecture, Simple call through a digital system, Common characteristics of digital switching systems Analysis Report. TEXT 2	7	L1,L2,L3.

5	**MAINTENANCE OF DIGITAL SWITCHING SYSTEM:** : Introduction, Scope, Software maintenance, Interface of a typical digital switching system central office, System outage and its impact on digital switching system reliability, Impact of software patches on digital switching system maintainability, methodology for reporting and correction of field problems Upgrade process success rate, Number of patches applied per year, Diagnostic resolution rate, Reported critical and major faults corrected, A strategy improving software quality. **ANALYSIS OF NETWORKED SWITCHING SYSTEMS :**Scope Switching in networked environment, network reliability requirements, current trends in DSS, future trends in DSS (TEXT 2)	8	L1,L2,L3

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3. Unit 4 – Digital Teaching and Learning.

Course Outcomes:

CO1 Demonstrate the understanding of basic fundamentals of a telecommunication and switching system.

CO2 Ability to Analyze traffic management and switching system.

CO3 Ability to describe the common switching & control techniques and switching system software.

CO4 Ability to describe the maintenance of digital switching systems and its controlling.

CO5 Ability to analyze the various types of connection and switching links used by industry for telecommunication system worldwide and recent and future trends in DSS

Cos	Mapping with POs	Mapping with PSOs
CO1	PO2,PO5,PO6,PO7,PO8,PO9,PO11,PO12	PSO1,PSO2,PS03
CO2	PO2,PO3,PO4, O5,PO6,PO7,PO8,PO9,PO11,PO12	PSO1,PSO2,PS03
CO3	PO2,PO3,PO4,PO6,PO7, PO8,PO9,PO11,PO12	PSO1,PSO2, PS03
CO4	PO4,PO6,PO7, PO8,PO9,PO11,PO12	PSO1,PSO2, PS03
CO5	PO3,PO4,PO6,PO7, PO8,PO9,PO11,PO12	PSO1,PSO2,PS03

Text Book:

1. **J E flood,** "Telecommunication Systems",", First Edition, Pearson Education, 2002
2. **Syed R Ali,** "Digital Switching Systems, edition, publisher, 2002

Reference Books:

1. **John C Bellamy ,** "Digital Telephony", 3rd , Wiley India, 2000
2. **A.Bar-Lev**, "Semiconductor and Electronic Devices", 3rd edition, PHI, 1993

Web Links:	
1.	1 http://nptel.ac.in/ online course /digital switching systems
2.	https://books.google.co.in/books/about/Digital_Switching_Systems K Chandrashekar''Digital Switching Systems
3.	https://www.youtube.com/watch?v=oOMlwW4rBz8/jeflood

Sub Title: Programming with Python		
Sub Code:18EC552	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Assignment + SEE = 40 + 5 +5+ 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understanding the basics and data structure- list, tuples, dictionaries
2. To understand the control flow, functions modules and error handling.
3. To understand the object oriented concepts in python.
4. To get familiarised in the concepts of decorators and regular expressions.
5. To work with files and data structures in python.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**Introduction:** Basics of Python Programming, Using the REPL(Shell), Running Python Scripts, Variables, Assignment, Keywords, Input- Output, Indentation. Data Types - Integers, Strings, Booleans **Operators and Expressions:** Operators- Arithmetic Operators, Relational Operators, Assignment Operators, Logical Operators, Bitwise Operators, Membership Operators, Identity Operators, Expressions and order of evaluations. **Data Structures:** Lists - Operations, Slicing, Methods; Tuples, Sets, Dictionaries, Sequences, Comprehensions. **Text1**	08	L1, L2, L3
2	**Control Flow** - if, if-elif-else, for, while, break, continue, pass. **Functions** - Defining Functions, Calling Functions, Passing Arguments, Keyword Arguments, Default Arguments, Variable-length arguments, Anonymous Functions, Fruitful Functions. **Modules**: Creating modules, import statement, from .import statement, name spacing, Programming Examples **Text1**	08	L1, L2, L3
3	**Object Oriented Programming in Python**: Creating a class, The Self Variable, Namespaces, Types of Methods, Inner classes Inheritance and Polymorphism: Constructors in Inheritance, The Super() Method, Types of Inheritance: Single/Multiple, Method Resolution order, Polymorphism, Operator Overloading, Method overloading, Method Overriding. Programming Examples **Text1**	08	L1, L2, L3
4	**Files in Python**: Types of files, Working with Text files, Working with Binary Files, Pickle Module. **Data Structures in Python**: Linked Lists, Stacks, Queues, Deques. Programming Examples **Text1**	07	L1, L2, L3
5	**Decorators:** Introduction, Decorating functions with Parameters, Chaining decorators in python, property decorator: Class without getters and setters, Class with getters and setters	08	L1, L2, L3

	Regular Expressions: Regular Expression, Sequence Characters in Regular Expression, Quantifiers in Regular Expression, Special characters in Regular Expression, Using Regular Expression on Files, Retrieving Information from HTML File, Programming Examples **Text1**		

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5
3. Group activity for a group of 4 or 5 students -5 marks
4. UNIT 1 - Digital teaching and learning

Course Outcomes

CO1. Demonstrate the understanding and usage of core python scripting elements, python constructs, data types, lists, tuples and dictionaries

CO2. Demonstrate the understanding and usage of control structures module and exception handling

CO3. Demonstrate usage of object oriented features such as Inheritance, Polymorphism, operator overloading

CO4. Apply the knowledge of python and use the language scripting elements and constructs to develop file handling and build the data structures

CO5. Apply the concept of decorators and regular expressions.

COs	Mapping with POs
CO1	PO5,PO6
CO2	PO5,PO6
CO3	PO5,PO6,PO7,PO8,PO9
CO4	PO5,PO6,PO7,PO8,PO9
CO5	PO5,PO6,PO7,PO8,PO9

TEXT BOOKS:

1. Core Python Programming: Dr.R.Nageshwara Rao, Dream Tech Press 2018

REFERENCE BOOKS/WEB LINKS:

1. Think Python, Allen Downey, Green Tea Press.
2. Core Python Programming, W.Chun, Pearson.
3. Introduction to Python, Kenneth A. Lambert, Cengage.
4. Learning Python, Mark Lutz, Orielly

EBOOKS:

1. http://greenteapress.com/wp/think- python
2. https://www.programiz.com/python-programming/decorator
3. https://www.programiz.com/python-programming/property

Sub Title : ARTIFICIAL NEURAL NETWORK		
Sub Code:EC553	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Assignment + SEE = 45 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To provide a strong foundation of fundamental concepts and structures in Neural Networks.
2. To understand the Analysis of different techniques and algorithms in Neural Networks.
3. To study the concepts of setting parameters and multilayered Networks.
4. To understand the concepts of Prediction, Polynomial Neural Networks.
5. To analyze the Optimization techniques in Neural Networks
6. To enable the student to apply these technique in applications which involve neural models.

UNIT No	Syllabus Content	No of Hours
1	Introduction, Fundamental concepts and models of Artificial Neural Network, Biological Neural Networks, structure and function of single neuron, neural network architectures, modelling of neural network, benefits of neural networks. Learning process. Supervised learning and Un-supervised learning.	08
2	Supervised Learning for single layer network: Perceptron, linear separability, Perceptron Training Algorithm, Delta rule, guarantees of success, modifications. Supervised Learning for Multi- layer network: multilevel discrimination, preliminaries, Back propagation, setting parameter values, theoretical results.	09
3	Prediction networks: Introduction, Recurrent network, William's and Zipser's Algorithm, Radial Basis Functions, Polynomial networks, Higher order network, Sigma–pi network, Function link architecture,Pi-sigma network, Regularization	08
4	Unsupervised learning: Winner take all networks. Hamming networks, Maxnet, Simple competitive learning, Hebb rule, Optimization Methods: Hop filed networks, Travelling Sales person problem, Solving simultaneous Liner equations, Allocating documents to multiprocessors, Iterated Gradient Descent	08
5	Case studies on neural network modelling: Application of MATLAB in Neural Network, UC Irvine Machine Learning Repository	06

Note 1: All Units will have internal choice.

Note 2: Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2. Assignment - 2 from units 3, 4 and 5.

Note 3 : Digital learning – Unit 05

Course Outcomes:

CO1. Understand the basic concepts of Neural Networks.
CO2. Analysis and development of different techniques in neural networks.
CO3. Analysis the concepts of Prediction Networks.
CO4. Understand and analysis of the concepts of Polynomial networks in Artificial
CO5. Analyze and design a real world problem for implementation and understand the dynamic behaviour of a system.
CO6. Use different optimization, machine learning technique for different model and enveloping the application.

Cos	Mapping with POs
CO1	P01,P02,P05,PO6
CO2	P02,P07
CO3	P08,P09
CO4	P09,P10
CO5	P07,P09

TEXT BOOKS:

1. Kishan Mehrotra, C. K. Mohan, Sanjay Ranka,Penram, **"Elements of Artificial Neural Networks"**, ***1997.***
2. J. Zurada, Jaico, **"Introduction to Artificial Neural Systems"**, ***2003.***

REFERENCE BOOKS/WEBLINKS:

1. Simon Hayking, **"Neural Networks: A Comprehensive Foundation",**2nd Edition, PHI.
2. Laurene Fausett, **"Fundamentals of Neural Networks: Architecture, Algorithms and Applications",** Person Education, 2004.

Sub Title : Object Oriented Programming with C++		
Sub Code: 18EC554	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE =40+ 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Listing OOPs concepts and recognizing the programming elements.
2. Developing and managing the object oriented programs.
3. Understanding the concepts of OOPS to develop the robust programs.
4. Understand and manage the error handling.
5. Understand Pointers

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Beginning with C++:** Basic concepts of object oriented programming, structure of C++ program, basic data types, user defined data types, derived data types, reference variables, operators in C++, scope resolution operator, memory management operators, manipulators, implicit conversions and control structures. **Functions in C++:** The main function, function prototyping, call by reference, return by reference, inline function, default arguments, const arguments, recursion, function overloading, Friend and virtual Functions TEXT-1	08	L1, L2, L3
2	**Classes and Objects*:*** C structures revisited, Specifying a class, Defining member function, A C++ program with class, making outside function inline, Nesting of member functions, private member function, Arrays with in a class, Memory allocation for the objects, static data members, static member functions, Array of objects, objects as function argument, Friend function, returning an object TEXT 1	06	L1,L2,L3
3	**Constructors and Destructors:** Constructors, Parameterized constructors, multiple constructors in a class, Constructors with default arguments, Dynamic initialization of objects, copy constructor, destructors. **Operator overloading:** Overloading of unary operators and overloading of Binary operators, overloading binary operators using friends**.** TEXT 1	09	L1,L2,L3,L4
4	**Inheritance:** Introduction, Defining derived classes, single inheritance, Making private function inheritable, multilevel inheritance, multiple inheritance, Hierarchical inheritance, Hybrid inheritance, virtual base class, abstract class	06	L1,L2,L3,L4

	TEXT 1		
5	**Exception Handling:** Introduction, basics of exception handling, Exception handling mechanisms, throwing mechanisms, catching mechanisms, Rethrowing an exception, specifying Exceptions, Exceptions in constructors and destructors. **Pointers, virtual functions and polymorphisms:** Introduction, pointers, pointers to objects, this pointer, pointers to derived classes, virtual functions, pure virtual functions, virtual constructors and destructors. TEXT 1	10	L1,L2,L3,L4

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.
Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.
Note 3.Unit 5 taught through Digital Learning.

Course Outcomes:

CO1. To gain the knowledge of object oriented concepts and get familiarized with basic concepts of programming.
CO2. Ability to design the programs using the classes and managing the objects.
CO3. Ability to design the programs with features of extensibility and use many operators.
CO4. Ability to develop the programs with reusability
CO5. Ability to develop the programs with built in error handling and use of pointers in the program

Cos	Mapping with POs
CO1	PO6
CO2	PO6
CO3	PO6
CO4	PO6, PO12
CO5	PO6, PO12

Text Book:

1.	**E. Balaguruswamy**," Object Oriented Programming with C++", fifth edition, Tata McGraw Hill, 2012.

Reference Books:

1.	**Stanley B.Lippmann, JoseeLajore**, "C++ Primer", 4th Edition, Addison Wesley, 2005.
2.	**Paul J Deitel, Harvey M Deitel**, "C++ for Programmers", edition, Pearson Education, 2009.
3.	**Herbert Schildt,** "The Complete Reference C++", 4th Edition, Tata McGraw Hill, 2003.

Web Links:	
1.	.https://www.tutorialspoint.com/cplusplus/cpp_object_oriented.htm
2.	.https://www3.ntu.edu.sg/home/ehchua/programming/cpp/cp3_OOP.html
3.	http://www.josuttis.com/cppbook/code.html

Subject Title : Control Systems

Sub.Code: 18EC555 No. of Credits: 03:00:0 (L - T – P) No. of Lecture Hours/Week : 03

Exam Duration: 03 Hrs CIE+Assignment +SEE=45+5+50=100 Total No.of Contact Hours:39

Course Learning Objectives:

1 Able to understand the basic concepts of Control systems, types and Transfer Functions.
2 Able to understand the Mathematical models and Analogy of Control Systems and analyze and evaluate the transfer functions using Block Diagram and Signal Flow Graphs.
3 Able to Understand, Analyse, evaluate the Time domain specifications for the second order systems using Step, ramp, impulse and parabolic functions as inputs to the second order systems.
4 Able to Examine and analyse the stability of control systems using time and frequency domain(graphical).
5 Able to understand the concept of state variables and analyse and evaluate the dynamic behaviour of control systems using state variables.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
1	**Introduction to Control systems:** Introduction**,** Types of Control systems, Effect of feedback systems and requirements of good control systems: **Mathematical Modeling of Control Systems:** Modeling of mechanical systems (Rotational and Translational excluding Lever and Gear trains systems). Transfer functions (Multivariable systems), Modeling of Electrical systems (Current and voltage analogy) Electromechanical Systems and its Analogous systems.	08	L1,L2,L3.L4
2	**Block diagrams:** Block diagram of a closed loop systems and its reduction techniques, Transfer Functions (Multivariable Systems), Applications of Block diagram *TEXT 1.* **Signal Flow Graphs:** Mason's gain formula, Basic properties of Signal flow graph, Transfer Functions-(Multivariable systems), Construction of Signal flow graph for closed loop control systems, and Applications of Signal Flow Graphs.	08	L1,L2,L3.
3	**Time Response of feedback control systems:** Time response of control systems**,** Standard test signals, Unit step response of First and Second order Systems. Time response specifications and its derivations, Time response specifications of second order systems, steady state errors and Error constants. Types of control systems(Steady state error for Type 0,1 and 2 systems) *TEXT 1.*	08	L1,L2,L3.

Unit No	Syllabus Contents	No.of Hours	Blooms Taxnomy level.
4	**Stability analysis:** Concepts of stability, Necessary conditions for Stability, Routh stability criterion, Difficulties in the formulation of the Routh table, Applications of Routh stability criterion only for linear feedback control systems, Relative stability analysis **Root Locus:** Introduction, Root locus concepts, Construction of Root loci, Rules for the construction of Root-Locus, Determination of roots for a specified open loop gain, Determination of Open loop gain for a specified damping of dominant roots, Numerical examples (Only for second order systems) *TEXT 1.*	08	L1,L2,L3.
5	**Frequency responses analysis:** Introduction, Frequency domain specifications (No derivations, Numerical examples),Bode plots, General procedure for constructing the Bode plots(Basic factors), Calculation of transfer function from Magnitude plot, Assessments of relative stability using Bode plots, Computation of Gain and Phase Margins from Bode plot, Gain adjustment in Bode Plot. *TEXT 1.*	07	L1,L2,L3.

Note 1: All the Units will have Internal Choice.

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2.

Assignment -2 from Units 3, 4 and 5

Note 3: Unit 4 will be taught through digital method.

Course Outcomes:

CO1 Ability to Develop and understand the Mathematical Model of Mechanical, Electrical and Electro Mechanical Systems, and also obtain the transfer function by using Block Diagram and Signal Flow Graphs.

CO2 Ability to Analyse and evaluate the first order and second order systems in time domain approach.

CO3 Ability to define, understand, analyse and evaluate the stability of a second order system in Time domain as well as frequency domain specifications.

CO4 Ability to Design and analyse the stability of the second order Control Systems using Root locus, Bode Techniques.

CO5 Ability to use Modern tools to obtain the state models for the electrical and Mechanical systems and evaluate their response in time domain as well as frequency approach.

Course Outcomes Mapping with Programme Outcomes.

CO1 PO1, PO2, PO3, PO11, PO12

CO2 PO1, PO2, PO3, PO11, PO12

CO3 PO1, PO2, PO3, PO11, PO12

CO4 PO1, PO2, PO3, PO11, PO12

CO5 PO1, PO2, PO3, PO11, PO12

Text Books.

1 J.Nagarath and M.Gopal, "Control Systems Engineering", 5th Edition, New Age International (P) Limited Publishers, 2005

Reference Text Books.

1 K.Ogata, "Modern Control Engineering", 4th Edition, Pearson Education Asia/PHI, 2002.

2 Benjamin C. Kuo, "Automatic Control Systems" , 9th Edition, John Wiley India Pvt. Ltd., 2008

3 Joseph J Distefano III et al., "Feedback and Control System", 2nd Edition, Schaum's Outlines, TMH, 2007.

Web Links.

1 https://www.electrical4u.com/mathematical-modelling-of-various-system/.

2 https://www.tutorialspoint.com/control_systems/control_systems_time_response_analysis.htm.

3 www.facstaff.bucknell.edu/mastascu/econtrolhtml/rootlocus/rlocus1a.html.

4 lpsa.swarthmore.edu/Bode/BodeExamples.html.

5 https://www.calvin.edu/~pribeiro/courses/engr332/Handouts/nyquist-margins.htm.

6 nptel.ac.in/courses/108103008/25.

Sub Title : Microcontroller Lab		
Sub Code: 18ECL56	**No. of Credits:1=0 : 0 : 1 (L-T-P)**	**No. of lecture hours/week : 02**
Exam Duration : 3 Hours	**CIE + SEE = 50 + 50 =100**	**Total No. of Contact Hours :26**

Course objectives:

1. 1. To learn the architecture of 8051 Microcontroller.
2. To learn the Instruction set and Embedded C for MCS51.
3. Ability to write a ALP and C program for a given algorithm and implement the same
4. To learn the I/O ports and interfacing techniques with MCS51.
5. Ability to develop single chip solution using MCS51.

Unit No.	Syllabus contents	No of Hours	RBT level
	PART-A **PROGRAMMING WITH 8051 MICROCONTROLLER**		
1.	**Data Transfer**: Block move, Exchange, Finding largest element in an array, sorting.	2	L1,L2,L3
2.	**Arithmetic Instructions**: Addition/subtraction, multiplication and division, square, Cube	3	L1,L2,L3
3.	**Counters:** 8/16 bit (Software)	2	L1,L2,L3
4.	**Boolean & Logical Instructions (Bit manipulations):** Logic gates, Adder/Subtractor, multiplexer circuits	2	L1,L2,L3
5.	**Code conversion**: BCD – ASCII; ASCII – Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX.	2	L1,L2,L3
6.	**Programs to generate time delay using** on-Chip timer/Counter, Program as event counter, Programs using serial port and Programs using interrupts.	2	L1,L2,L3
	PART B **INTERFACING PROGRAMS:**		
1.	Program to display BCD UP counting	2	L1,L2,L3
2.	DAC interfacing(square, triangular and ramp)	2	L1,L2,L3
3.	Program to control the stepper motor	4	L1,L2,L3
4.	Program to display the key pressed	2	L1,L2,L3
5.	LCD interfacing		L1,L2,L3

Course Outcomes:

CO1. Understand the architectural features of microcontrollers.
CO2. Explain the instruction sets of Microcontrollers and write Assembly and High level Programs.
CO3. Study the various features of Microcontrollers based systems.
CO4. Study the applications of Microcontrollers for real time systems.
CO5. Development of single chip solutions

Cos	Mapping with POs
CO1	PO2, PO3
CO2	PO2, PO3

CO3	PO2, PO3, PO11, PO12
CO4	PO2, PO3, PO11, PO12
CO5	PO2, PO3, PO11, PO12

Text Book:	
1.	**Kenneth J, Ayala**, "The 8051 Microcontroller Architecture, Programming & Applications", 2edition, 1996 / Thomson Learning 2005.
2.	**Muhammad Ali Mazidi, Janice Gillespie Mazidi and Rollin D. McKinlay,** "The 8051 Microcontroller and Embedded Systems – using assembly and C",; PHI, 2006 / Pearson, 2006.

Sub Title : Digital Signal Processing Laboratory		
Sub Code: 18ECL57	**No. of Credits:1=0 : 0 : 1 (L-T-P)**	**No. of lecture hours/week : 02**
Exam Duration : 3 Hours	**CIE + SEE = 50 + 50 =100**	**Total No. of Contact Hours :26**

Course Objectives:

1. To analyze the sampling process, impulse response, convolution, frequency domain response
2. of LTI systems
3. To analyze and design digital IIR and FIR filters
4. To demonstrate the DSP algorithms using Matlab software
5. To demonstrate the DSP algorithms using Code Composer Studio

Unit No.	Syllabus contents	No of Hours	RBT level
1.	**Matlab Programs** 1. Verification of sampling theorem. 2. Impulse response of a given system 3. Linear convolution of two given sequences. 4. Circular convolution of two given sequences 5. Autocorrelation of a given sequence and verification of its properties. 6. Cross correlation of given sequences and verification of its properties. 7. Solving a given difference equation. 8. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum. 9. Linear convolution of two sequences using DFT and IDFT. 10. Circular convolution of two given sequences using DFT and IDFT 11. Design and implementation of FIR filter to meet given specifications. 12. Design and implementation of IIR filter to meet given specifications. . **TEXT 1 and TEXT2**	24	L1, L2,L3
2.	**Hardware experiments** 1. Linear convolution of two given sequences. 2. Circular convolution of two given sequences. 3. Computation of N- Point DFT of a given sequence 4. Noise: Add noise above 3 KHz and then remove; Interference suppression using 400 Hz tone. 5. Impulse response of first order system. **TEXT 2**	12	L3,L4, L5

NOTE: Experiments from1 to 5 will be taught by digital and online platform.

Course Outcomes:

CO1	Define and verify the sampling theorem, impulse response, convolution and frequency response of the system
CO2	Understand DFT, IDFT, Auto correlation and Cross correlation
CO3	Analyze and design digital IIR and FIR filters.
CO4	Demonstration of DSP algorithms using Matlab software.
CO5	Demonstration of DSP algorithms using Code Composer Studio software.

Course Outcomes Mapping with Programme Outcomes.

CO1	PO1,PO2,PO3,PO4,PO5, PO12	PO11,
CO2	PO1,PO2,PO3,PO4,PO5, PO12	PO11,
CO3	PO1,PO2,PO3,PO4,PO5, PO12	PO11,
CO4	PO1,PO2,PO3,PO4,PO5, PO12	PO11,
CO5	PO1,PO2,PO3,PO4,PO5, PO12	PO11,

Text Books.

1 Sanjeet K. Mitra, “Digital Signal Processing using MATLAB”, Edition, TMH, 2001

2 B. Venkataramani and Bhaskar, “Digital Signal Processors”, edition, TMH, 2002

Reference Text Books.

1 J. G. Proakis & Ingale, “Digital Signal Processing using MATLAB”, edition, Mc Graw Hill, 2000

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2018 Batch)

VI Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing/ Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	PC	18HS61	Management and Entrepreneurship	EC	03	--	--	03	050	050	100	03
2	PC	18EC61	CMOS VLSI Design	EC	04	--	--	04	050	050	100	04
3	PC	18EC62	Embedded Systems	EC	03	--	--	04	050	050	100	03
4	PC	18EC63	Computer Communication Network	EC	04	--	--	04	050	050	100	04
5	PC	18EC64x	Professional Elective – 2	EC	03	--	--	03	050	050	100	03
6	PC	18ECExx	Open Elective –B	EC	03	--	--	03	050	050	100	03
7	PC	18ECL66	Embedded Systems Laboratory	EC	--	--	02	02	050	050	100	01
8	PC	18ECL67	VLSI Laboratory	EC	--	--	02	02	050	050	100	01
9	PC	18ECP68	Mini Project					03	050	050	100	02
10	INT	18EC169	Internship	To be carried out during the intervening vacations of VI an VII semesters				--	--	--	--	--
				Total	**20**	**00**	**04**	**27**	**450**	**450**	**900**	**24**

18EC65x_Professional Elective – 2 (PECEL 2)		
Sl. No.	**Course Code**	**Course Title**
1	18EC641	Semiconductor Fabrication
2	18EC642	Cryptography
3	18EC643	Information Theory & Coding
4	18EC644	System Verilog for verification
5	18EC645	Internet of Things

Open Elective-B(OE-B)		
Sl. No.	**Course Code**	**Course Title**
1	18ECE05	Automotive Safety Measurements(ME,IEM,EE)
2	18ECE06	Nano Electronics (CS,IS,ML,TC)
3	18ECE07	Wireless Sensor Networks(EE,ML,EI)
4	18ECE08	Robotics and Machine vision systems(ME,EI,EE,ML)

BOS Chairman Dean(Academics) Principal

Sub Title : CMOS VLSI DESIGN		
Sub Code: 18EC61	**No. of Credits:4=4 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : 3 Hours	**CIE +Assignment + SEE = 45 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. Impart knowledge of MOS transistor theory and CMOS technologies
2. Learn the operation principles and analysis of inverter circuits, Understand basic circuit concepts and scaling of MOS circuits.
3. Representation of different forms of diagrams like layout & stick diagram.
4. Different CMOS logic structures
5. Analyze adder & multiplier circuits, Design Combinational, sequential and dynamic logic circuits as per the requirements.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**MOS Transistor theory:** Enhancement and Depletion mode operation MOS transistors (p & n type), MOS fabrication (p & n type), CMOS fabrication. MOS device design equations, Second order effects of MOS, Static CMOS Inverter DC Characteristics, Beta Ratio Effect, Noise Margin, Pass Transistor, Transmission Gate, Tristate Inverter. **Scaling of MOS Circuits:** Scaling models and scaling factors, Scaling factors for device parameters, Limitation of Scaling (Points). **(Text 1, 2)**	10	L1,L2
2	**Circuit Design Processes:** MOS layers, Stick diagrams, Design rules and layout, lambda-based design rules. **Basic Circuit Concepts:** Sheet resistance, Area capacitances, Capacitance calculations, the delay unit, Inverter delays, driving capacitive loads. **(Text 1)**	9	L1, L2
3	**CMOS Logic Structures:** CMOS Complementary Logic, Pseudo-nMOS Logic, Dynamic CMOS Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS Domino Logic, BiCMOS logic, Cascaded Voltage Switch Logic (CVSL). **(Text 2, 3).**	10	L1,L2,L3

4	**Datapath Subsystem I:** Single bit addition, carry generation & propagation, PG Carry-Ripple Addition, Manchester carry chain adder, carry skip adder, carry select, conditional sum adders. **DataPath Subsystems II:** Unsigned Array Multiplication, 2's Complement Array Multiplication (Modified Baugh-Wooley two's complement Multiplier), Booth encoding (Radix 4). **(Text 3).**	11	L1,L2
5	**Sequential MOS Logic Circuitry:** SR Latch Circuitry, Clocked latch and Flip Flop Circuitry, CMOS D-Latch and Edge Triggered Flip-Flop. **(Text 4)**	12	L1,L2,L3

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.
Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.
Note 3. Unit 5- Digital Teaching and Learning.

Course Outcomes:

CO1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling
CO2. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
CO3. Describe different logic structures.
CO4. Design of Adder and Multiplier circuits using MOS transistors
CO5. Demonstrate ability to design Combinational, sequential and dynamic logic circuits.

Cos	Mapping with POs
CO1	PO1,PO2,PO3,PO5
CO2	PO1,PO2,PO3
CO3	PO1,PO2,PO3
CO4	PO1,PO2,PO3
CO5	PO1,PO2,PO5

Text Book:

1.	**Douglas A Pucknell & Kamran Eshragian**, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994).
2.	**Neil H. E. Weste, and David Money Harris** , "CMOS VLSI Design- A Circuits and Systems Perspective", 4th Edition, Pearson Education.
3.	**Neil H.E Weste, David Harris, Ayan Banerjee,** "CMOS VLSI design- A circuits and systems perspective", Third edition Pearson Education (Asia) Pvt. Ltd, 2006
4.	**Sung Mo Kang & Yosuf Leblebici**, "CMOS Digital Integrated Circuits: Analysis and Design" -, Third Edition, Tata McGraw-Hill.

Reference Books:	
1.	**R. Jacob Baker**, "CMOS Circuit Design, Layout and Simulation", edition, John Wiley India Pvt. Ltd, year
2.	**Behzad Razavi,** "Design of Analog CMOS Integrated Circuits", TMH, 2007.

Web Links:	
1.	http://nptel.ac.in

Subject Title : Embedded Systems		
Sub. Code: 18EC62	**No. of Credits:04=04:0:0 (L -T – P)**	**No. of Lecture Hours/Week : 03**
Exam Duration: 03 Hrs	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours:39**

Course objectives:

1. Understand the basic concepts of Embedded Systems.
2. Explain the Characteristics and quality attributes and Program of Embedded Systems.
3. Get exposure to an advanced microcontroller Cortex M3.
4. Understand the definition, structure and Working of Real Time Operating system.
5. Analyze different Embedded Systems in various Domain applications.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Typical Embedded System:** Definition, Embedded systems vs. General Computing Systems, Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components, PCB and Passive Components. TEXT 1	10	L1,L2,L3.
2	**Characteristics and Quality Attributes of Embedded Systems:** Characteristics of an Embedded system, Quality attributes of Embedded Systems. **Hardware Software Co-Design and Program Modelling:** Fundamental issues in Hardware Software Co-Design, Computational Models in Embedded Design. **Embedded firmware Design and Development:** Embedded firmware design approaches, Embedded firmware development languages. TEXT 1	07	L1,L2,L3.
3	**ARM-32 bit Microcontroller:** ARM Cortex-M3 Processor-Introduction, Overview of the Cortex-M3, Cortex-M3 Basics, Instruction Sets. TEXT 2	07	L1,L2,L3.
4	**RTOS for Embedded System Design:** Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Multiprocessing and Multitasking, Task scheduling, Task Communication, Task Synchronisation, Device Drivers, How to choose an RTOS. TEXT 1	08	L1,L2,L3.
5	**Trends in the Embedded Industry:** Processor trends in embedded system, Embedded OS trends, Development Language Trends, Open Standards, Frameworks and Alliances, Bottlenecks. **Embedded Systems-Application and Domain Specific**: Washing Machine-application specific Embedded System, Automotive-Domain Specific Example of Embedded Systems, Key Players of Automotive Embedded Market. **Design Case Studies**: Digital camera, Embedded Systems in Automobile, Smart Card Reader, Automated Meter Reading System.	07	L1,L2,L3.

	TEXT 1		

Note 1.Unit 1, 2, 3, 4 and 5 will have internal choice.
Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.
Note 3. Unit 4-Digital Teaching and Learning.

CO1. Understand different blocks of a Typical Embedded System.
CO2. Analyse different characteristics, quality attributes and modelling Techniques of embedded system design
CO3. Apply the knowledge of Instruction Set to program ARM 32 bit Microcontroller.
CO4. Analyze the concepts of Real time kernel & Operating System services.
CO5. Evaluate the current trends in embedded industry and analyse different application and domain specific examples of embedded systems through case studies.

COs	**Mapping with POs**
CO1	PO1,PO3
CO2	PO1,PO2,PO3,PO4,PO5
CO3	PO1,PO2,PO3,PO4,PO5,PO6
CO4	PO1,PO2,PO3,PO4,PO5
CO5	PO1,PO2,PO3,PO4,PO5,PO6

Text Book:

1.	Shibu K V, "Introduction to Embedded Systems", First Edition, Tata McGraw Hill Education Private Limited, 2009
2.	Joseph Yiu, "The Definitive Guide to the ARM Cortex-M3", Second Edition, Newnes, (Elsevier), 2008

Reference Books:

1.	Raj Kamal, "Embedded Systems – Architecture, Programming and Design", edition, Mc Graw Hill, 2012
2.	James K Peckol "Embedded Systems – A contemporary Design Tool", edition, John Weily, 2008

Web Links:

1.	https://onlinecourses.nptel.ac.in/noc20_cs15/course

Sub Title: Computer Communication Networks		
Sub Code:18EC63	**No. of Credits:4=4: 0: 0 (L-T-P)**	**No. of lecture hours/week: 4**
Exam Duration: 3 hours	**CIE +Assignment + SEE = 45 + 5 + 5+50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. Insight into the basics of networking, OSI reference and TCP/IP model.
2. Study of access links, protocols, error detection and correction techniques in the data link layer.
3. Understanding of router, routing algorithms, addressing techniques of the network layer.
4. Reliable data transfer, multiplexing, demultiplexing and congestion control techniques of the transport layer.
5. Services, Protocols, directory service and Sockets of the application layer

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Basics of computer Communications Network:** Network Components, Representations, Data Flow, Protocol Layers and their Service Models, Network Addressing, Network topologies, Network connecting devices, Network types. Text1, Text2	10	L1, L2, L3
2	**The Link Layer: Links, Access Networks, and LANs:** Introduction to the Link Layer, Error-Detection and Correction Techniques, Multiple Access Links and Protocols, Switched Local Area Networks, Link Virtualization: A Network as a Link Layer Text1	10	L1, L2, L3
3	**The Network Layer:** Introduction, Virtual Circuit and Datagram Networks, What's Inside a Router? The Internet Protocol (IP): Forwarding and Addressing in the Internet, Routing Algorithms, Routing in the Internet, Broadcast and Multicast Routing Text1	11	L1, L2, L3
4	**Transport Layer:** Introduction and Transport-Layer Services, Multiplexing and De-multiplexing, Connectionless Transport: UDP, Principles of Reliable Data Transfer, Connection-Oriented Transport: TCP, Principles of Congestion Control, TCP Congestion Control. Text1	11	L1, L2, L3
5	**Application Layer:** Principles of Network Applications, The Web and HTTP, File Transfer: FTP, Electronic Mail in the Internet, DNS—The Internet's Directory Service, Peer-to-Peer Applications, Socket Programming. Text1	10	L1, L2, L3

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From unit 1 and 2, Assignment2 from units 3,4 and 5
3. Group activity for a group of 4 or 5 students -5 marks
4. UNIT 1 - Digital teaching and learning

Course Outcomes

CO1	Define the network components, layers, addressing, topology, connectivity and network types for data transmission.
CO2	Distinguish the basic network configurations and standards associated with each network.
CO3	Describe the layering architecture of computer networks and distinguish between the OSI reference model and TCP/IP protocol suite.
CO4	Identify the protocols and functions associated with the transport layer services.
CO5	Construct a network model and determine the routing of packets using different routing algorithms

COs	Mapping with POs
CO1	PO2, PO3, PO4
CO2	PO2, PO3, PO4, PO5
CO3	PO2, PO3, PO4, PO5, PO12
CO4	PO2, PO3, PO4, PO5, PO12
CO5	PO2, PO3, PO4, PO5, PO12

Text Book:

1. James F. Kurose, Keith W. Ross, "**Computer Networks**", Pearson Education, 2nd Edition, **2003**.
2. B.Forouzan ," **Data Communication and Networking**", TMH, 4th Edition, ***2006***. CCNA routing and Switching study guide.
3. James F. Kurose, Keith W. Ross, "**Computer Networks**", Pearson Education, 2nd Edition, **2003**.

Reference Books:

1. Russel Bradford, "**The Art of Computer Networking"**, Pearson Education, I st Edition, **2007**.

MOOCS:

1. nptel.ac.in/courses/106105081/1
2. http://www.bau.edu.jo/UserPortal/UserProfile/PostsAttach/10617_1870_1.pdf

Sub Title : Semiconductor Fabrication		
Sub Code: 18EC641	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Assignment + SEE = 45 + 05 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To be able to understand Scope of semiconductor Materials and Devices.
2. To be able to understand the Process of Crystal Growth.
3. To be able to understand the Photolithography and Etching.
4. To be able to classify the Diffusion and Ion Implantation.
5. To be able to understand the Film Deposition and Process Integration.

UNIT No	Syllabus Content	No of Hours
1	**Introduction to Semiconductor:** semiconductor Materials, Devices, Semiconductor process technology-key semiconductor technology, technology trends. Basic Fabrication Steps-oxidation, photolithography, etching, diffusion, Ion Implantation and metallization. **Text1**	7
2	**Crystal Growth:** Silicon crystal growth from the melt-starting material, czochralski technique, distribution dopant, effective segregation coefficient. Silicon float zone process. GaAs crystal growth techniques- starting materials, crystal growth techniques. Material characterization- wafer shaping, crystal characterization. **Silicon Oxidation:** Thermal oxidation process-kinetics of growth, thin oxide growth. Impurity redistribution during oxidation, Masking properties of silicon dioxide, oxide quality, oxide thickness characterization. **Text1**	8
3	**Photolithography and Etching:** Optical Lithography- the clean room, exposure tools, masks, photo resist, pattern transfer and resolution enhancement technique. **Etching:** Wet chemical etching-Si etching, Silicon dioxide etching, silicon Nitride and poly silicon etching, Aluminum etching and GaAs etching. Dry etching- Plasma Fundamentals, Etch mechanism. **Text1**	8
4	**Diffusion and Ion Implantation:** Basic Diffusion Process- Diffusion Equation, Diffusion profiles. Extrinsic Diffusion and Lateral diffusion. **Introduction Ion Implantation:** Range of Implanted Ions- Ion Distribution, Ion Stopping, Ion Channeling. Implant Damage and Annealing- Implant Damage, Annealing. **Text1**	8
5	**Film Deposition and Process Integration:** Epitaxial Growth Techniques- Chemical Vapor Deposition. Structures and Defects in Epitaxial Layers, Dielectric Deposition- Si Dioxide, Si Nitride. Poly silicon Deposition. Metallization- Physical Vapor Deposition and Aluminum Metallization and copper Metallization.	8

	Text1	

Note 1: All the units will have internal choice.

Note 2: Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1: Identify the Semiconductor Materials.
CO2: Ability to interpret Fabrication Steps.
CO3: Creation of semiconductor devices
CO4: Ability to Compare the types of Diffusion and Ion Implantation.

Cos	Mapping with POs
CO1	PO5,PO7,PO8
CO2	PO7,PO8,PO10
CO3	PO5,PO8,PO12
CO4	PO5,PO9,PO11

TEXT BOOK:

1. Gary S. May, Simon M. Sze, **"Fundamentals of Semiconductor Fabrication"** Wiley, 1st Edition, 2003.

REFERENCE BOOKS/WEBLINKS:

1. Anderson, Anderson" **Fundamentals of Semiconductor Devices**" McGraw-Hill Education, Indian Edition 2013.
2. Gary S. May, Costas J S, **"Fundamentals of Semiconductor Manufacturing and Process Control**" Wiley IEEE Press, 1st Edition, 2006

Sub Title : Cryptography		
Sub Code: 18EC642	**No. of Credits:3=3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Assignment + SEE = 45 + 05 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To impart the basic concepts of network security and classical encryption, number theory, stream ciphers, block ciphers and authentication
2. To interpret the cryptographic algorithms like stream ciphers and block ciphers using classical encryption techniques
3. To apply the concept of classical encryption techniques to stream ciphers and block ciphers
4. To analyse the stream ciphers, block ciphers and authentication functions
5. To design the stream ciphers, block ciphers and authentication functions

UNIT No	Syllabus Content	No of Hours
1	**Introduction:** Services, mechanisms and attacks, OSI security architecture, Model for network security. **Symmetric ciphers:** Symmetric Cipher Model, Substitution Techniques: Caesar Cipher, Mono Alphabetic Cipher, Playfair Cipher, Hill Cipher, polyalphabetic Cipher and One-Time Pad (OTP). Transposition Techniques, Rotor Machines, Steganography.	08
2	**Finite Fields:** Groups, Rings, Fields. Modular Arithmetic: Divisors, properties of modulo operator, modular arithmetic operations and properties. Euclid's Algorithm, Greatest Common Divisor (GCD), finding GCD. Finite Fields of the form GF (p): Finite fields of order p, finding multiplicative inverse in GF (p).	08
3	**Private Key Encryption:** Simplified DES, Block Cipher Principles, Data encryption standard (DES), Strength of DES, Block Cipher Design Principles and Block Cipher Modes of Operation, Evaluation Criteria for Advanced Encryption Standard, The AES Cipher.	08
4	**Public Key Encryption:** Principles of Public-Key Cryptosystems, The RSA algorithm. Key Management, Diffie - Hellman Key Exchange.	08
5	**Authentication Functions and Hash Functions:** Authentication functions, message authentication codes, hash functions, security of Hash functions and MACs	07

Note 1: All the units will have internal choice.

Note 2: Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1 - Define the basic concepts of network security, classical encryption, number theory, Private key, public key, authentication.

CO2 -Understand the structure of cryptographic algorithms and their applications.

CO3 -Apply the concept of classical encryption techniques to existing standard algorithms.

CO4 -Illustrate the significance of cryptographic algorithms and their applications.

CO5 -Design the private key and public key, authentication functions for applications.

Cos	Mapping with POs
CO1	PO1,PO2,PO10,P12
CO2	PO1,PO2,PO10,P12
CO3	PO1,PO2, PO3, PO10,P12
CO4	PO1,PO2, PO3, PO10,P12
CO5	PO1,PO2,PO10,P12

TEXT BOOK:

1. William Stallings, Cryptography & Network Security – Principles and Practice, 5th Edition, Pearson, 2011.

REFERENCE BOOKS/WEBLINKS:

1. Behrouz Forouzan, Cryptography and Network Security, 2nd Edition, TMH, 2010
2. Alfred J. Menezes, Paul C. Van Oorschot and Scott A. Vanstone, Handbook of Applied Cryptography, CRC Press, Reprint 2001.
3. Bruce Scheiner, Applied cryptography: protocols, algorithms, and source code in C, 2nd Edition, Wiley, 2008.

Web Links:

1. http://www.nptel.ac.in/courses/106105031/
2. http://faculty.mu.edu.sa/public/uploads/1360993259.0858Cryptography%20and%20Network%20Security%20Principles%20and%20Practice,%205th%20Edition.pdf

Sub Title : INFORMATION THEORY AND CODING		
Sub Code: 18EC643	**No. of Credits:03=03:0:0 (L :T :P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives: This course will enable students

1. To understand the basic concepts of information theory.
2. To study and analyze the several source encoding algorithms.
3. Analyze the fundamental limits on performance of a communication system.
4. Study the different error control coding techniques.
5. Analyze the various types of binary cyclic codes.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**INFORMATION THEORY:** Introduction, Measure of information, Average information content of symbols in long independent sequences, Average information content of symbols in long dependent sequences. Markoff statistical model for information source, Entropy and information rate of mark-off source. TEXT 1	08	L1,L2, L3
2	**SOURCE CODING:** Encoding of the source output, Shannon's encoding algorithm, Source coding theorem, Huffman coding.(Only binary codes) TEXT 1	06	L2,L3,L4
3	**FUNDAMENTAL LIMITS ON PERFORMANCE:** Communication Channels: Discrete communication channels, Continuous communication channels. Discrete memory less Channels, Mutual information, Channel Capacity, Channel coding theorem, Channel capacity Theorem. TEXT 1 and TEXT 2	08	L2,L3,L4
4	**Topic to be covered under Digital learning** **INTRODUCTION TO ERROR CONTROL CODING:** Introduction, Types of errors, examples, Types of codes, Linear Block Codes: Matrix description, Error detection and correction, Standard arrays and table look up for decoding. TEXT 1 and TEXT 2	09	L1,L2,L3,L4
5	**BINARY CYCLE CODES**: Algebraic structures of cyclic codes, Encoding using an (n-k) bit shift register, Syndrome calculation. BCH codes, RS codes, Golay codes, Turbo codes, LDPC codes. TEXT 1	08	L1,L2,L3,L4

Note 1.Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2 Assignment - 2 from units 3, 4 and 5.

Note 3.Unit 4 (Introduction to Error control coding) will be taught using Digital learning platform.

Course Outcomes:

CO1: Understand the concepts of information theory, source coding, channel coding, error control coding and binary cyclic codes.

CO2: Apply information theory to source coding, channel coding and error control coding.

CO3: Evaluate Entropy, Average code Length, Source coding efficiency and Channel capacity.

CO4: Analyze Various types of errors and coding techniques.

CO5: Design source encoder and syndrome calculation circuits.

Cos	Mapping with POs
CO1	PO1,PO2,PO8
CO2	PO1,PO2,PO3,PO8
CO3	PO1,PO2,PO3,PO8
CO4	PO1,PO2,PO3,PO8
CO5	PO1,PO2,PO8

Text Book:	
1.	K. Sam Shanmugam,"Digital and Analog communication systems ", Second Edition, John Wiley India Pvt, 1996
2.	Simon Haykins, "Digital communication", Second edition, John Wiley India Pvt. Ltd, 2008

Reference Books:	
1.	J. Das, S. K. Mullick, P. K. Chatterjee ,"Principles of digital communication",Wiley, 1986 - Technology & Engineering
2.	P.S Satyanarayana, "Information Theory and Coding", edition, Dyanaram Publications, Reprint 2001
3.	Giridhar, "Information Theory and Coding", 2nd edition, Pooja Publications, 2006
4.	Ranjan Bose, "Information Theory and coding and Cryptography", 2nd edition, TMH, 2009

Sub Title: System Verilog for verification		
Sub.Code: 18EC644	No. of Credits:3=3:0:0 (L - T – P)	No. of Lecture Hours/Week : 03
Exam Duration:03 Hrs	CIE+Assignment +SEE=45+5+50=100	Total No.of Contact Hours:39

Course objectives:

1. Insight to apply System Verilog concepts to do synthesis, analysis and architecture design.
2. Understanding of System Verilog and SVA for verification, and understand the improvements in verification efficiency.
3. Analyze coverage driven verification for given design under test (DUT).
4. Understand advanced verification features, such as the practical use of classes, randomization, checking, and coverage.
5. Knowledge to communicate the purpose and results of a design experiment in written and oral presentations.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Verification Guidelines:** Introduction, Verification Process, Verification Plan, Verification Methodology Manual, Basic Test bench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage. **Text 1**	08	L1, L2, L3
2	**Data Types:** Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Creating New Types with typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings. **Text 1**	07	L1, L2, L3
3	**Basic Object Oriented Programming:** Where to Define a Class, OOP Terminology, Understanding Dynamic Objects. **System Verilog Assertions**: Types of Assertions and examples. **Text 1**	08	L1, L2, L3
4	**Threads and Inter-process Communication:** Working with Threads, Inter-process Communication, Events, Semaphores, Mailboxes, Building a Test bench with Threads and IPC Functional Coverage: Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Coverage Options, Parameterized Cover Groups. **Text 1 and Text 2**	08	L1, L2, L3, L4
5	**Introduction to formal verification:** Introduction to formal techniques and property specification, Reachability analysis, Elements of property languages, Property language layers, PSL basics, Formal test plan process. **Text 2 and Text 3**	08	L1, L2, L3

Note 1.Two assignments are evaluated for 5 marks
Note 2.Group activity is evaluated for 5 marks.
Note 3.Unit-5-Digital learning and teaching.

Course Outcomes

CO1. Use System Verilog to create correct, efficient, and re-usable models for digital designs.
CO2. Use System Verilog to create test benches for digital designs.
CO3. Understand and effectively exploit new constructs in System Verilog for verification.
CO4. Use of threads and inter-process communication for system Verilog.
CO5. Understand the process of formal verification.

COs	Mapping with POs
CO1	PO2, PO3, PO4
CO2	PO2, PO3, PO4, PO5
CO3	PO2, PO3, PO4, PO5, PO12
CO4	PO2, PO3, PO4, PO5, PO12
CO5	PO2, PO3, PO4, PO5, PO12

Text Book:	
1.	Chris Spear, "**System Verilog for Verification: A Guide to Learning the Test bench Language Features"**, Springer 2006.
2.	Janick Bergeron, **"Writing Test benches Using System Verilog**", Springer, 2006.
3.	Stuart Sutherland, Simon Davidman and Peter Flake, **"System Verilog for Design: A Guide to Using System Verilog for Hardware Design and Modeling**", 2nd Edition, Springer.

Reference Books:	
1.	Janick Bergeron, **"Writing Test benches: Functional Verification of HDL Models**", Second edition, Kluwer Academic Publishers, 2003.
2.	Mark Glasser, **"Open Verification Methodology Cookbook**", Springer, 2009.
3.	Andreas S. Meyer, **"Principles of Functional Verification**", Elsevier Science, 2004.
4.	Harry D. Foster, Adam C. Krolnik, David J. Lacey, "**Assertion-Based Design**", 2nd Edition, Kluwer Academic Publishers, 2004.

MOOCS:

1. ElectronicDesignAutomationhttp://nptel.ac.in/courses/106105083/
2. DigitalsystemdesignwithPLDsandFPGAshttp://nptel.ac.in/courses/117108040/ Fundamentals of HDL (Lecture #008)
3. https://www.youtube.com/watch?v=rdAPXzxeaxs&index=8&list=PLE3BC3EBC9CE 15FB0

Subject Title : Embedded Systems Lab		
Sub. Code: 18ECL67	**No. of Credits: 1 = 0:1:0 (L - T – P)**	**No. of Lecture Hours/Week : 02**
Exam Duration:03 Hrs	**CIE +SEE = 50 + 50 = 100**	**Total No.of Contact Hours: 24**

Course objectives:

1. To study the features of LPC 1768 MCU.
2. Develop the Assembly level programming of ARM Cortex M3 Processor.
3. Develop the Embedded C level programming of ARM Cortex M3 Processor.
4. Understand Interfacing of different modules to LPC 1768 MCU.
5. Develop 32-bit microcontroller based Embedded system applications.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	Write a Assembly language program to link Multiple object files and link them together.	2	L1, L2, L3, L4
2	The Assembly language program i. To calculate the value of the function. ii. To store data in desired Memory location.	2	L1, L2, L3, L4
3	The Assembly language program 1. To calculate the 2's Complement of a number. 2. To calculate the Square of a number .	2	L1, L2, L3, L4
4	Write a C program to Output the message using UART of LPC1768.	2	L1, L2, L3, L4
5	Write a C Program to interface LED using LPC 1768.	2	L1, L2, L3, L4
6	Write a C Program to interface Relay using LPC 1768.	2	L1, L2, L3, L4
7.	Write a C Program for DC motor/Stepper motor rotation using LPC 1768.	2	L1, L2, L3, L4
8.	Write a C program to interface a Real Time Clock (RTC) of LPC 1768.	2	L1, L2, L3, L4
9	Write a program to read on-chip ADC value and display it on UART terminal using LPC 1768.	2	L1, L2, L3, L4
10	.Write a C programs to interface a DAC of LPC 1768.	2	L1, L2, L3, L4
11	Write a C program to demonstrate the use of an External interrupt in LPC 1768	2	L1, L2, L3, L4
12	Write a C program to interface Keypad using LPC 1768.	2	L1, L2, L3, L4

CO1. Understanding features of the architecture of ARM Cortex M3.
CO2. Understanding features of the architecture of LPC 1768 MCU

CO3. Write assembly level programs to program ARM Cortex M3

CO4. Interface different modules to LPC 1768 MCU.

CO5. Design and testing a program for Different Embedded applications.

COs	**Mapping with POs**
CO1	PO1, PO2,PO3, PO9
CO2	PO1, PO2,PO3 PO9
CO3	PO1, PO2, PO3, PO5, PO9
CO4	PO1, PO2, PO3, PO5,PO9
CO5	PO1, PO2, PO3, PO5,PO9

Reference Books:	
1.	Shibu K V, **"Introduction to Embedded Systems"**, First Edition, Tata McGraw Hill Education Private Limited, 2009
2.	Joseph Yiu, "**The Definitive Guide to the ARM CORTEX-M3**", Second Edition, Newnes , **2008**
3.	NXP Semiconductors, "**LPC17xx user manual**",
4.	Micro-CM3768, "**ARM Cortex-M3 Development Board User Manual**

Note: Programming to be done in **Keil µvision-5** IDE tool and download the program on to a Cortex-M3 evaluation board **NXP LPC1768** using **Flash Magic Tool.**

Web Links:	
1.	https://www.youtube.com/watch?v=nyUry1o2SQQ&list=PLnFckqm074doPiUQkkhwpHzP0JI7tAg4p

Subject Title : CMOS VLSI DESIGN LAB		
Sub. Code: 18ECL67	**No. of Credits: 1 = 0:1:0 (L - T – P)**	**No. of Lecture Hours/Week : 02**
Exam Duration:03 Hrs	**CIE +SEE = 50 + 50 = 100**	**Total No. of Contact Hours: 24**

Course objectives:

1. Design, model, simulate and verify CMOS digital circuits
2. Design layouts CMOS digital circuits
3. Perform physical verification of CMOS digital circuits
4. Perform RTL- flow and understand the stages in ASIC design.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	DC, Transient analysis of CMOS logic-Universal gates schematic	2	L1, L2, L3, L4
2	DC, Transient analysis of CMOS full adder schematic	2	L1, L2, L3, L4
3	DC, Transient analysis of Pass transistor and transmission gates schematic	2	L1, L2, L3, L4
4	DC, Transient analysis of Sequential circuits schematic 1. Clocked D Latch 2. Master-Slave Edge Triggered Register	2	L1, L2, L3, L4
5	DRC and LVS analysis of CMOS Inverter layout	2	L1, L2, L3, L4
6	DRC and LVS analysis of Common Source Amplifier Layout	2	L1, L2, L3, L4
7.	DRC and LVS analysis of Common Drain Amplifier Layout	2	L1, L2, L3, L4
8.	DRC and LVS analysis of Differential Amplifier Layout	2	L1, L2, L3, L4
9	Synthesis and Simulation of Inverter using Verilog code	2	L1, L2, L3, L4
10	Synthesis and Simulation of Buffer Verilog code	2	L1, L2, L3, L4
11	Synthesis and Simulation of Basic/Universal Gate using Verilog code	2	L1, L2, L3, L4
12	Synthesis and Simulation of JK, MSJK flip-flops using Verilog code	2	L1, L2, L3, L4

CO1. Design and simulate basic CMOS circuits like different logic structures.
CO2: Design and simulate basic CMOS circuits like inverter, common source amplifier and

Differential Amplifier.

CO3: Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list.

CO4: Design and simulate combinational and sequential digital circuits using Verilog HDL.

COs	Mapping with POs
CO1	PO1, PO2,PO3, PO9
CO2	PO1, PO2,PO3 PO9
CO3	PO1, PO2, PO3, PO5, PO9
CO4	PO1, PO2, PO3, PO5,PO9

Text Books:	
1.	**Douglas A Pucknell & Kamran Eshragian**, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994).
2.	**Neil H. E. Weste, and David Money Harris** , "CMOS VLSI Design- A Circuits and Systems Perspective", 4th Edition, Pearson Education.
3.	**Neil H.E Weste, David Harris, Ayan Banerjee,** "CMOS VLSI design- A circuits and systems perspective", Third edition Pearson Education (Asia) Pvt. Ltd, 2006
4.	**Sung Mo Kang & Yosuf Leblebici**, "CMOS Digital Integrated Circuits: Analysis and Design" -, Third Edition, Tata McGraw-Hill.

Note: Digital Teaching and Learning: DRC and LVS analysis of Differential Amplifier Layout.

Software required: Cadence/or any other equivalent software

Web Links:	
1	http://nptel.ac.in

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2021-22

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2018 Batch)

VII Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	MC	18HS71	Cost Management of Engg Projects	HS	03	--	--	03	050	050	100	02
2	PC	18EC71	Wireless Communication	EC	04	--	--	03	050	050	100	04
3	PC	18EC72	Microwave and Antenna	EC	04	--	--	03	050	050	100	04
4	PE	18EC73X	Professional Elective-3	EC	03	--	--	03	050	050	100	03
5	PE	18EC74X	Professional Elective-4	EC	03	--	--	03	050	050	100	03
6	OE	18EC75X	Open Elective-C	EC	03	--	--	03	050	050	100	03
7	PC	18ECL76	Advance Communication Lab	EC	--	--	02	02	050	050	100	01
8	PC	18ECL77	Computer Communication Network Lab	EC	--	--	02	02	050	050	100	01
9	Project	18ECP78	Project work phase-1	EC	--	--	02	02	050	050	100	02
10	INT	18ECI79	Internship	--	--	--	--	---	---	---	--	--
				Total	**20**	**--**	**06**	**24**	**400**	**400**	**800**	**23**

Internship: All the students admitted to III year of BE have to undergo mandatory internship of 4 weeks during the vacations of VI and VII semesters and /or VII and VIII semesters. A University examination will be conducted during VIII semester and prescribed credit are added to VIII semester. Internship is considered as a head of passing and is considered for the award of degree. Those, who do not take-up/complete the internship will be declared as failed and have to complete during subsequent University examination after satisfy the internship requirements

Note: : PC: Professional Core. PE: Professional Elective, OE: Open Elective. MC: Mandatory Course, PRJ: Project work, INT: Internship

Select **ANY ONE** of the Professional Elective. Open Elective-A: Students can select any one of the open electives (Please refer to consolidated list of Dr AIT for open electives) offered by any Department

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2021-22

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2018 Batch)

Professional Elective-3(PE-3)		
Sl. No.	**Course Code**	**Course Title**
1	18EC731	5G Technology
2	18EC732	Virtual Reality
3	18EC733	Real Time Operating systems
4	18EC734	DSP Algorithm and architecture
5	18EC735	Network and Cyber Security
6	18EC736	Optical Fibre Communication

Professional Elective-4(PE-4)		
Sl. No.	**Course Code**	**Course Title**
1	18EC741	Analog and Mixed Mode VLSI
2	18EC742	Operating systems
3	18EC743	Satellite Communication
4	18EC744	Real Time Embedded Systems
5	18EC745	Operations Research
6	18EC746	Adaptive Signal Processing

Open Elective-C (OE-C)		
Sl. No	**Course Code**	**Course Title**
1	18EC751	Internet of Things (CS, IS, EI, TE, ML, ME, IEM, EEE, CV)
2	18EC752	Cryptography (CS, IS, ML,TE, EI,EEE)
3	18EC753	Mobile Communication (EI, EE, ML)
4	18EC754	Bio Mechatronics (CS, IS, EI, TE, ML, ME, IEM, EEE, CV)
5	18EC755	Introduction to Unmanned Aerial Vehicle (UAV) (CS,IS, EI, TE,ML, ME, IEM, EEE,CV)

BOS Chairman Dean(Academics) Principal

Professional Elective-3(PE-3)		
Sl. No.	**Course Code**	**Course Title**
1	18EC731	5G Technology
2	18EC732	Speech and Audio Processing
3	18EC733	Real Time Operating systems
4	18EC734	DSP Algorithm and architecture
5	18EC735	Network Security

Professional Elective-4(PE-4)		
Sl. No.	**Course Code**	**Course Title**
1	18EC741	Analog and Mixed Mode VLSI
2	18EC742	Operating systems
3	18EC743	Satellite Communication
4	18EC744	ASIC Design
5	18EC745	Operational Research

Open Elective-C(OE-C)		
Sl. No	**Course Code**	**Course Title**
1	18ECE09	Internet of Things (CS,IS,EI,ML)
2	18ECE10	Cryptography and Network Security(CS,IS,ML,TC)
3	18ECE11	Mobile Communication(EI,EE,ML)
4	18ECE12	High Speed Electronics(EE,EI,ML,TC)

Sub Title: WIRELESS COMMUNICATION		
Sub Code:18EC71	**No. of Credits:4=4: 0: 0 (L-T-P)**	**No. of lecture hours/week: 4**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. Understand the basics of wireless communication used for mobile telephony
2. Apply the basic methodologies of cellular system designing.
3. Describe the 3G network architecture and cellular network
4. Understand GSM and TDMA technologies and GSM Call establishment, Cal handoff and Roaming
5. Distinguish between CDMA technology, wireless LAN and PAN technologies

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	Introduction to wireless telecommunication systems and Networks, History and Evolution of wireless radio system, Development of modern telecommunication infrastructure, overview of existing Network infrastructure, Wireless Network applications, Future Wireless Network. Different generations of wireless cellular networks 1G, 2G,2.5G ,3G and 4G Cellular system and beyond, Wireless standard organizations. **TEXT 1**	10	L1,L2,L3.
2	Common Cellular System components, Common cellular network components, Hardware and software, views of cellular networks, 3G cellular systems components. Cellular component identification, Call establishment. **TEXT 1**	10	L1,L2,L3
3	Wireless network architecture and operation: The cellular concept Cell fundamentals, Capacity expansion techniques, Cellular backhaul networks, Mobility management, Radio resources and power management, Wireless network security.**TEXT1**	10	L1,L2,L3.
4	GSM and TDMA Technology: GSM system overview-introduction to GSM and TDMA,GSM Network and System Architecture, GSM channel concept, GSM system operations-GSM identities, GSM system operations (Traffic cases). **TEXT1**	11	L1,L2,L3,L4
5	CDMA Technology: CDMA system overview, introduction to CDMA,CDMA network and system architecture CDMA basics: CDMA Channel concept, CDMA operations(Layer 3) 3g CDMA,IS95B,CDMA 2000 and WCDMA Wireless LANs/IEEE 802.11X: Introduction and Evolution of Wireless LANs, Design issues.	11	L1,L2,L3,L4,L6

	Wireless PAN/IEEE 802.15x: Introduction, Wireless Pan application and Architecture. **TEXT1**		

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

Course Outcomes:

CO1: Understand and Identify the telecommunication system and networks system, Different generations of wireless cellular networks 1G, 2G,2.5G ,3G and 4G Cellular system and beyond, Wireless standard organizations.

CO2: Analyze Common Cellular System components, Common cellular network components, Hardware and software views of cellular networks.

CO3: Understand Wireless network architecture and operation, power management and network security and Capacity expansion techniques,.

CO4: Understand GSM and TDMA Technologies. GSM frame concept , GSM system operation registration, call setup, location updating, and call hand off procedure,

CO5: Analyze the design issues in CDMA, Wireless LAN and PAN Networks 3G cellular system components; list the components of wireless cellular network and different frequency band used in GSM and CDMA

COs	Mapping with POs
CO1	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12
CO2	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12
CO3	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12
CO4	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12
CO5	PO1, PO2,PO3,PO5,PO8,PO9,PO10,PO12

Text Books.

1. Garry J Mullet, "Introduction to Telecommunication Systems and Networks: , India Edition, Delmar Cengage Learning,2007

Reference Text Books.

1. T L Singal, "Wireless Communications", Tata McGraw-Hill, Education, 2010
2. Vijay K Garg, "IS-95 CDMA and cdma2000: Cellular/PCS Systems Implementation", Pearson Education, reprint 2006

Web Links.

1. http://www.nptel.ac.in /courses/117102062/

Sub Title : Microwave and Antenna		
Sub Code: 18EC72	**No. of Credits:4=4 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 04**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :52**

Course objectives:

1. Understanding the basics of microwave and waveguides.
2. Understanding the concepts of microwave networks, microwave passive devices and semiconductor devices.
3. Understanding microwave tubes, microwave design principles and antenna basics.
4. Understanding the importance of point sources, arrays and radiations from wires.
5. To understand different types of antennas like aperture, reflector, broadband and Microstrip antennas.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction to Microwaves** -History of Microwaves, Microwave Frequency bands, applications of Microwaves, Losses associated with microwave transmission, Concept of Impedance in Microwave transmission. **Waveguides-** Rectangular waveguide, Circular waveguide, Strip line, Micro strip line. **TEXT 1,2**	09	L1, L2, L3.
2	**Microwave Network Analysis -** Network parameters for microwave circuits, Scattering Parameters. **Microwave Passive devices and semiconductor Devices -** Microwave passive devices - Directional Coupler, Power Divider, Magic Tee, Attenuator, Resonator. Microwave Semiconductor Devices - Gunn Diodes, IMPATT diodes, PIN diodes**. TEXT 1,2**	09	L1, L2,L3
3	**Microwave Tubes:** Klystron- two cavity klystron amplifier and reflex klystron (klystron oscillator) **Microwave Design Principles -** Microwave Filter Design, RF and Microwave Amplifier Design **Antenna Basics -** Physical concept of radiation, near and far field regions, basic antenna parameters: radiation patterns, beam area, radiation Intensity, beam efficiency, reciprocity, directivity and gain, antenna apertures, effective height, bandwidth, radiation efficiency, radio communication Link, antenna temperature and antenna field zones. **TEXT 1,2,3.4**	11	L1,L2,L3
4	**Radiations from wires:** Short electric dipole, fields of a short dipole, radiation resistance of dipole, Half wave dipole antenna, folded dipole antennas. **Point Sources & their arrays -** Arrays, Point source, Power theorem and its application, Examples of power patterns, Field patterns, Phase patterns, Array of isotropic point sources different cases, non-isotropic sources, principle of pattern multiplication, linear arrays of n elements of equal amplitude & spacing, broad side, end fire arrays **TEXT 3,4**	11	L1,L2,L3,L4

5	**Aperture and Reflector Antennas**- Huygens' principle, radiation from rectangular and circular apertures, design considerations, Babinet's principle, Radiation from sectoral and pyramidal horns, design concepts, prime-focus parabolic reflector and cassegrain antennas. **Broadband Antennas**- Log-periodic and Yagi-Uda antennas, frequency independent antennas, broadcast antennas. **Micro strip Antennas**- Basic characteristics of micro strip antennas, feeding methods, methods of analysis, design of rectangular and circular patch antennas. **TEXT 3.4**	12	L1,L2,L3,L4

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2. Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3. Unit 1- Digital Teaching and Learning

Course Outcomes: After the completion of the Course the student can:

CO1. Identify the microwave frequency band, its applications and different types of waveguides
CO2. Analyze microwave networks, microwave passive devices and semiconductor devices.
CO3. Apply microwave design principle, microwave tubes and antenna basics.
CO4. Be able to analyze the radiation patterns from different types of wires, point sources and their arrays.
CO5. Illustrate and design antennas like aperture, reflector, and broadband. Microstrip antenna.

Cos	Mapping with POs	Mapping with PSOs
CO1	PO1,PO2,PO8,PO9	PSO1,PSO2,PS03
CO2	PO1,PO2,PO4,PO8,PO9,PO12	PSO1,PSO2,PS03
CO3	PO1,PO2,PO3,PO4,PO5,PO7,PO8,PO9,PO12	PSO1,PSO2, PS03
CO4	PO1,PO2,PO3,PO4,PO5,PO6,PO7,PO8,PO9,PO12	PSO1,PSO2, PS03
CO5	PO1,PO2,PO3,PO4,PO5,PO6,PO7,PO8,PO9,PO12	PSO1,PSO2, PS03

Text Book:	
1.	Collin RE. **Foundations for microwave engineering**. John Wiley & Sons; 2007.
2.	Annapurna Das, Sisir K Das, **Microwave Engineering,** TMH Publication, 2001
3.	J.D. Kraus**, Antennas**, McGraw Hill, 1988.
4.	C.A. Balanis, **Antenna Theory** - Analysis and Design, John Wiley, 1982.

Reference Books:	
1.	Microwave Devices and circuits- Liao / Pearson Education. 1992
2.	M.Kulkarni., "Microwave devices and Radar Engg."Umesh Publications, 2011
3.	R.E. Collin, Antennas and Radio Wave Propagation, McGraw Hill, 1985.
4.	I.J. Bahl and P. Bhartia, Micro Strip Antennas, Artech House, 1980.

Web Links:	
1.	www.nptel.in
2.	https://www.academia.edu/12559664/Collin_Foundations_for_Microwave_Engineering
3.	https://www.academia.edu/13759443/Basic_Antennas_Understanding_Practical_Antennas_and_Design_Joel_R_Hallas_2009
4.	www.youtube/microwave , www.youtube/antennas

Sub Title: 5G Technology		
Sub Code:18EC731	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hrs	**CIE +Assignment+Group Activity + SEE = 40 + 5 +5+ 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Assess the genesis and impact of 5G and use case requirement in real world.
2. Understanding the 5G architecture and its deployment.
3 Understanding the security features in 5G technology..
4. Understanding the wireless spectrum crunch 5G technologies.
5. Analyzing and understanding SON and Green flexible RF in 5G technology.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**Drivers for 5G: The 'Pervasive Connected World'** Introduction, Historical Trend of Wireless Communications, Evolution of LTE Technology to Beyond 4G, 5G Roadmap, 10 Pillars of 5G, 5G in Europe, 5G in North America, 5G in Asia, 5G Architecture**Text1**	08	L1, L2, L3
2	**The 5G Internet Introduction,** Internet of Things and Context- Awareness, Internet of Things, Context- Awareness, Networking Reconfiguration and Virtualization Support, Software Defined Networking, Network Function Virtualization, Mobility, An Evolutionary Approach from the Current Internet, A Clean- Slate Approach, Quality of Service Control, Emerging Approach for Resource Over- Provisioning **.Text1**	08	L1, L2, L3
3	**Security for 5G Communications:** Introduction, Overview of a Potential 5G Communications, System Architecture, Security Issues and Challenges in 5G Communications Systems, User Equipment, Access Networks,, Mobile Operator's Core Network, External IP Networks **Text1**	08	L1, L2, L3
4	**The Wireless Spectrum Crunch: White Spaces for 5G?.** Introduction, Background, Early Spectrum Management, History of TV White Spaces, History of Radar White Spaces, TV White Space Technology, Standards, Approaches to White Space, White Space Spectrum Opportunities and Challenges, TV White Space Applications, International Efforts, Role of WS in 5G Text1	07	L1, L2, L3

5	**SON Evolution for 5G Mobile Networks,** Introduction, SON in UMTS and LTE, The Need for SON in 5G, Evolution towards Small- Cell Dominant HetNets, Towards a New SON Architecture for 5G, **Green Flexible RF for 5G:** Introduction, Radio System Design, Nonlinear Crosstalk in MIMO Systems **Text1**	08	L1, L2, L3

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5
3. Group activity for a group of 4 or 5 students -5 marks
4. UNIT 1 - Digital teaching and learning

Course Outcomes

CO1. Introduction to drivers in 5G technology.

CO2. Analyze the 5G architecture and its deployment.

CO3. Elaborate security features in 5G technology.

CO4. Analyze the role of wireless spectrum crunch 5G technologies.

CO5. Elaborate the SON and Green flexible RF in 5G technology.

COs	Mapping with POs
CO1	**PO1,PO2,PO8,PO12**
CO2	**PO1,PO3,PO8,PO12**
CO3	**PO1,PO6,PO8,PO12**
CO4	**PO1,PO3,PO8,PO12**
CO5	**PO1,PO2,PO8,PO12**

TEXT BOOKS:

1. **Jonathan Rodriguez**, "Fundamentals of 5G Mobile", Wiley Publications, 2015.

REFERENCE BOOKS/WEB LINKS:

1. **Afif Osseran, Jose F.Monserrat, Patrick Marsch,** " 5G Mobile and Wireless Communications Technology" Cambridge University Press, 2016
2. **Harri Holma, Antti Toskala, Takehiro Nakamura**, " 5G Technology: 3GPP New Radio", John Wiley & Sons Ltd. 2020

Sub Title: VIRTUAL REALITY		
Sub Code:18EC732	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To become familiar with the basic concepts of virtual reality Technology and input devices
2. To understand the output devices.
3. To study the concepts of Modeling in virtual
4. To understand the human factors in VR
5. To become familiar with the applications of VR

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**INTRODUCTION:** The three I's of virtual reality, commercial VR technology and the five classic components of a VR system. Input Devices: (Trackers, Navigation, and Gesture Interfaces): Three dimensional position trackers, navigation and manipulation, interfaces and gesture interfaces. **Text book1: 1.1, 1.3, 1.5, 2.1, 2.2 and 2.3**	09	L1,L2,L3
2	**OUTPUT DEVICES**: Graphics displays, sound displays & haptic feedback. **Text book1: 3.1,3.2 and 3.3**	07	L1,L2,L3,L4
3	**MODELING:** Geometric modeling, kinematics modeling, physical modeling, behavior modeling, model management. **Text book1: 5.1, 5.2 and 5.3, 5.4 and 5.5**	08	L1,L2, L3,L4
4	**HUMAN FACTORS:** Methodology and terminology, user performance studies, VR health and safety issues. **Text book1: 7.1, 7.2 and 7.3**	07	L1,L2,L3.
5	**APPLICATIONS:** Medical applications, military applications, robotics applications. **Text book1: 8.1, 8.3 and 9.2**	08	L1,L2, L3

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

Course Outcomes:

CO1: Describe the basic concepts of virtual reality and input devices.

CO2: Compare the input and output devices

CO3: Use the virtual reality modeling techniques

CO4: Illustrate the human factors in virtual reality

CO5: Understanding and identifying the applications of virtual reality

COs	Mapping with POs
CO1	PO1,PO2,PO4,PO5,PO8, PO12
CO2	PO2,PO3,PO4,PO5,PO10,PO12
CO3	PO1,PO2,PO3,PO5,PO6,PO7,PO12
CO4	PO1,PO2,PO4,PO5,PO11,PO12
CO5	PO1,PO2,PO5, PO11,PO12

Text Books.

1. Virtual Reality Technology, Second Edition, Gregory C. Burdea & Philippe Coiffet, John Wiley & Sons. 2003
2. Introduction to Virtual Reality, John Vince, Springer, London, Springer-Verlag London Limited 2004

Reference Text Books.

1. Virtual Reality Systems. John Vince, Pearson Education, 2007

Web Links.

1. https://doi.org/10.1007/978-0-85729-386-2, 978-1-85233-739-1
2. www.nptelcoursematerial
3. www.youtube/virtual
4. Introduction - Learning Virtual Reality [Book] (oreilly.com)
5. https://www.geeksforgeeks.org/virtual-reality-introduction

Sub Title : Real Time Operating System		
Sub Code: 18EC733	**No. of Credits:3=3: 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. study the basic concepts of specialized processors
2. study the various Scheduling strategies
3. study multi-resource services
4. study the embedded system components
5. understand design trade-offs

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction to real-time embedded systems:** Brief history of real time systems, a brief history of embedded systems. **System Resources:** resource analysis, real-time service utility, scheduling classes, the cyclic executive, scheduler concepts, preemptive fixed priority scheduling policies, Real-Time OS, thread safe reentrant functions. Text1	08	L1,L2
2	**Processing**: preemptive fixed-priority policy, feasibility, rate monotonic least upper bound, necessary and sufficient feasibility, deadline – monotonic policy, dynamic priority policies. **I/O Resources**: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture. Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems. Text1	08	L1, L2, L3
3	**Multi-resource Services**: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion. Soft Real-Time Services: Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services. Text1	08	L1, L2
4	**Embedded system components**: firmware components, RTOS system software mechanisms, software application components. **Debugging components:** exceptions assert, checking return codes, single-step debugging, kernel scheduler traces, test access ports, trace ports, power-on self test and diagnostics, external test equipment, application-level debugging. Text1	08	L1, L2
5	**High availability and reliability design:** reliability and availability, similarities and differences, reliability, reliable software, available software, design trade- offs, hierarchical applications for fail-safe design. Text1	07	L1, L2

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3.Unit 4---digital teaching and learning.

Course Outcomes:

CO1: Understand the basics of Real Time Embedded System and System Resources

CO2: Analyse the concepts Processing and IO Resources

CO3: Analyse Various multi-resource services

CO4: Analyse different Embedded System Components and Debug components.

CO5: Analyze and Categorize the design trade-offs

Cos	Mapping with POs
CO1	PO1, PO2
CO2	PO2, PO6
CO3	PO2,PO6, PO10,P12
CO4	PO2,PO6, PO10,P12
CO5	PO2,PO6, PO10,P12

Text Book:	
1.	Sam Siewert, "**Real-Time Embedded Systems and Components**," Cengage Learning India Edition, **2007**.
2.	John Wiley, **"Programming for Embedded Systems"**, Dreamtech SoftwareTeam, India Pvt. Ltd.,2008.

Reference Books:	
1.	Raj Kamal, "**Embedded Systems**", Tata McGraw Hill, New Delhi, ***2008***.
2.	Phillip. A. Laplante, "**Real-Time Systems Design and Analysis**", Prentice Hall India,2nd Edition, ***2005***.
3	Jane. W. S. Liu, "**Real Time Systems**", Pearson Education, ***2005***

Sub Title : DSP Algorithms and Architecture		
Sub Code: 18EC734	**No. of Credits:3=3: 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. To gain the knowledge of basics of DSP like DFT, FFT, LTI systems, Digital Filters.
2. To understand the architectures of DSP processors.
3. To study the implementation of DSP algorithms.
4. To understand the interfacing of DSP processors with memory and I/O devices.
5. To study the applications of DSP processor.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction to Digital Signal Processing:** Introduction, a Digital Signal-Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. **Architectures for Programmable Digital Signal Processors:** Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing. TEXT 1	09	L1,L2
2	**Programmable Digital Signal Processors:** Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54xx., Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and Programming, On-Chip peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor. TEXT 1	08	L1, L2
3	**Implementation of Basic DSP Algorithms:** Introduction, The Q-notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). TEXT 1	06	L2, L3,L4
4	**Implementation of FFT Algorithms:** Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit-Reversed Index Generation & Implementation on the TMS32OC54xx. **Interfacing Memory and Parallel I/O Peripherals to DSP Devices:** Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface,	10	L2, L3,L4

	Programmed I/O, Interrupts and I / O Direct Memory Access (DMA). TEXT 1		
5	**Interfacing and Applications of DSP Processor:** Introduction, Synchronous Serial Interface, A CODEC Interface Circuit. DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System. TEXT 1	06	L3,L4.L5

Note 1: Unit 1, Unit 2, Unit 3, Unit 4 and Unit 5 will have internal choice

Note 2: Two assignments are evaluated for 5 marks: Assignment -1 from Units 1 and 2. Assignment -2 from Units 3, 4 and 5.

Course Outcomes:

CO1: Define the fundamentals of DSP and the general architecture of DSP

CO2: Understand the general architecture of DSP processor and in particular TMS320C54xx DSP to run algorithms.

CO3: Applying the concept of DSP algorithms.

CO4: Analyse the implementation of FFT algorithms and interfacing memory to DSP processor.

CO5: Creating new designs based on existing algorithms targeted to DSP processor.

Cos	Mapping with POs
CO1	PO2, PO3, PO4, PO5,PO11,PO12
CO2	PO2, PO3, PO4, PO5,PO11,PO12
CO3	PO2, PO3, PO4, PO5,PO11,PO12
CO4	PO2, PO3, PO4, PO5,PO11,PO12
CO5	PO2, PO3, PO4, PO5,PO11,PO12

Text Book:

1. Avatar Singh and S. Srinivasan, "Digital Signal Processing", Third Edition, Thomsoc Learning, 2004

Reference Books:

1. Ifeachor E. C., Jervis B. W Pearson-Education, "Digital Signal Processing: A Practical Approach", edition, Pearson Education, 2002
2. B Venkataramani and M Bhaskar, "Digital Signal Processors", 2nd edition, TMH, 2010
3. Peter Pirsch, "Architectures for Digital Signal Processing", 4th edition, John Wiley, 2007

Web Links:

1. http://bwrcs.eecs.berkeley.edu/Classes/CS252/Notes/Lec09-DSP.pdf
2. http://nptel.ac.in/courses/117102060/

Sub Title: NETWORK AND CYBER SECURITY		
Sub Code:18EC735	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Assignment+ Group Activity + SEE = 40 + 5 +5+ 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Know about security concerns in Email and Internet Protocol. ·
2. Understand cyber security concepts. ·
3. List the problems that can arise in cyber security. ·
4. Discuss the various cyber security frame work.
5. Will be in a position to apply the concepts of cyber security framework in computer system administration.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**Transport Level Security:** Web Security Considerations, Secure Sockets Layer, Transport Layer Security, HTTPS, Secure Shell (SSH) Text 1:	08	L1, L2
2	**E-mail Security**: Pretty Good Privacy, S/MIME, Domain keys identified mail (Text1)	08	L1, L2
3	**IP Security**: IP Security Overview, IP Security Policy, Encapsulation Security Payload (ESP), Combining security Associations Internet Key Exchange. Cryptographic Suites (Text 1:)	08	L1, L2, L3
4	**Cyber network security concepts**: Security Architecture antipattern: signature based malware detection versus polymorphic threads, document driven certification and accreditation, policy driven security certifications. Refactored solution: reputational, behavioural and entropy based malware detection. The problems: cyber antipatterns concept, forces in cyber antipatterns, cyber anti pattern templates, cyber security antipattern catalog (Text-2)	07	L1, L2, L3
5	**Cyber network security concepts:** Enterprise security using Zachman framework Zachman framework for enterprise architecture, primitive models versus composite models, architectural problem solving patterns, enterprise workshop, matrix mining, mini patterns for problem solving meetings. (Text-2: Chapter 3 & 4).	08	L1, L2, L3

Note:

1. **Unit 1,2,3,4, and Unit 5 will have the internal choice**
2. **Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5**
3. **Group activity for a group of 4 or 5 students -5 marks**
4. **UNIT 1 - Digital teaching and learning**

Course Outcomes

CO1. Explain network security protocols ·

CO2. Understand the basic concepts of cyber security ·

CO3. Discuss the cyber security problems ·

CO4. Explain Enterprise Security Framework ·

CO5. Apply concept of cyber security framework in computer system administration.

COs	Mapping with POs
CO1	PO5,PO6
CO2	PO5,PO6
CO3	PO5,PO6,PO7,PO8,PO9
CO4	PO5,PO6,PO7,PO8,PO9
CO5	PO5,PO6,PO7,PO8,PO9

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325- 1877-3.
2. 2. Thomas J. Mowbray, "Cyber Security – Managing Systems, Conducting Testing, and Investigating Intrusions", Wiley.

REFERENCE BOOKS/WEB LINKS:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

Sub Title: Optical Fiber Communication		
Sub Code:18EC736	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understand the basic concept of adaptive filter and adaptive system
2. Identify the geometrical significance of Eigenvectors and values
3. Analyse the Simple, Newton's and Steepest Descent Gradient search method to search performance surface
4. Study estimation of LMS algorithm
5. Familiar with design of adaptive communication system, adaptive noise canceller and adaptive modeling in FIR digital filter synthesis

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**OVERVIEW OF OPTICAL FIBER COMMUNICATION:** Introduction, Historical development, general system, advantages, disadvantages, and applications of optical fiber communication, optical fiber waveguides, Ray theory transmission: total internal reflection, acceptance angle, numerical aperture , skew rays, Cylindrical fiber: modes, mode coupling, step index fibers and graded index fibers, single mode fibers: cutoff wave length and mode filed diameter. **TEXT 1**	07	L1.L2.L3
2	**TRANSMISSION CHARACTERISTICS OF OPTICAL FIBERS:** Introduction, Attenuation, Material absorption: Intrinsic and extrinsic absorption, linear scattering losses: Rayleigh scattering and Mie scattering, Dispersion: Chromatic dispersion: Material and Waveguide dispersion, bending loss. . **TEXT 1**	07	L1.L2.L3,L4
3	**OPTICAL FIBERS AND CABLES:** Cable design: Fiber buffering, cable structural and strength members, cable sheath and water barrier, examples of fiber cables. **OPTICAL SOURCES AND DETECTORS: Laser** :Introduction, basic concepts: absorption and emission of radiation, population inversion. Optical emission from semiconductors: The p-n junction, spontaneous emission, carrier recombination, stimulated emission and lasing, heterojunctions, semiconductor materials. **LED:** Introduction, power & efficiency: double heterojuncation LED **Detectors:** Introduction, quantum efficiency, responsivity. Semiconductor photodiodes: p-i-n and Avalanche photodiode, Phototransistors, photoconductive detectors. **TEXT 1**	09	L1.L2.L3,L4
4	**DIGITAL TRANSMISSION SYSTEMS:** Point –to-point links: System considerations, Link power Budget, Rise Time Budget, First window transmission distance, Transmission distance	07	L1.L2.L3

	for single mode Links **TEXT 2**		
5	**OPTICAL NETWORKS:** Introduction, Optical networks concepts: Optical networking terminology, Optical network node and switching elements, Optical network transmission modes, layers and protocols: Synchronous networks, Asynchronous transfer mode, internet protocol, Optical network deployment: Long haul networks, Metropolitan area networks, Access networks, Local area networks. Optical Ethernet, Network protection, restoration and survivability. TEXT 1	09	L1.L2.L3

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

Course Outcomes

CO1	Describe the basic concepts of propagation of optical energy in single and multimode optical fibers.
CO2	Compare the fiber losses and its measurements to provide background for optical fiber communications.
CO3	Use the cable design and Identify the optical sources and detectors.
CO4	Illustrate the digital transmission system of optical fiber communication
CO5	Understanding and Identifying the different optical Networks and its communication.

COs	**Mapping with POs**
CO1	PO1,PO2,PO4, PO12
CO2	PO2,PO3,PO4,PO10,PO12
CO3	PO1,PO2,PO3,PO6,PO7,PO12
CO4	PO1,PO2,PO4,PO11,PO12
CO5	PO1,PO2,PO11,PO12

Text Books.

1 John M. Senior, "**Optical Fiber Communications**", 3rd Impression Reprint v, Pearson Education, 2012

2 Gerd Keiser, "**Optical Fiber Communication**", 3rd Ed.,, MGH, Reprint, 2012

Reference Text Books.

1 Joseph C Palais, "**Fiber Optic Communication**", 4th Edition, Pearson Education, 2012

2 GowerJohn , "Optical Communication System", second edition, Prentice, 2013

Web Links.

1 www.google.com, Optical Fiber Communications", John M. Senior pdf
2 www.google.com, optical fiber communication gerd keiser 4th edition pdf
3 www.nptelcoursematerial
4 Nptel.ac.in/lectures/courses/117101002
5 www.youtube/opticalfibercommunication

Sub Title : Analog and Mixed Mode VLSI Design		
Sub Code: 18EC741	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understand the concept of Analog Design.
2. Analysis of Single stage amplifiers in VLSI perspective.
3. Analysis of Current sources and sinks in VLSI perspective.
4. Understand the concept of Data Converter Fundamentals.
5. Design and Mismatch Error Analysis of DAC and ADC Architectures.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Basic MOS Device Physics:** General considerations: MOSFET as a Switch, MOSFET Structure, MOS symbols, MOS I/V Characteristics: Threshold Voltage, Derivation of I/V Characteristics, Second Order Effects, MOS Device Models: MOS Device Layout, capacitances, MOS Small-signal Model, NMOS versus PMOS devices, Long-channel vs Short-channel devices.**(Text 1)**	09	L1,L2,L3
2	**Single Stage Amplifiers:** Basic Concepts, Common source stage, Common Source stage with resistive load, Common Source stage with Diode connected load, Common Source Stage with Current Source load, Common Source stage with Triode load, Common Source stage with source degeneration. **(Text 1)**	07	L1, L2,L3
3	**Current Sources and Sinks:** The current mirror, The Cascade Connection, Sensitivity Analysis, Transient response, other current sources & sinks. **(Text 1, 2)**	07	L2,L3,L4
4	**Data Converter Fundamentals:** Analog versus Digital discrete time signals, Converting Analog signals to Digital signals, Sample and Hold Characteristics, DAC specifications, ADC specifications, Mixed signal layout issues. **(Text 2)**	07	L2,L3,L4
5	**Data Converter Architectures:** DAC architecture, Digital input code, Resistors string, R-2R ladder networks, Current steering, Charge scaling DACs, Cyclic DAC, Pipeline DAC. **ADC Architecture:** Flash, 2-step flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC. **(Text 2)**	09	L2,L3,L4

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Course Outcomes:

CO1. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
CO2. Ability to Analyse and Design of Single Stage Amplifiers.
CO3. Ability to Analyse and Design of Current sources and sinks.
CO4. Understand concepts of ADC and DAC
CO5. Analysis of ADC, DAC Architectures and Mismatch errors.

Cos	Mapping with POs
CO1	PO3, PO4
CO2	PO4, PO5
CO3	PO5, PO7
CO4	PO10, PO12
CO5	PO3, PO12

Text Book:	
1.	Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Twenty Fifth Reprint, TATA McGraw Hill, 2013.
2.	R Jacob Baker, "CMOS Circuit Design, Layout and Simulation", PHI, 2005.

Reference Books:	
1.	Philip E Allen and Douglas R Holberg, "CMOS Analog Circuit Design", Second edition, Oxford University Press, 2004.
2.	Adel Sedra and K C Smith, "Microelectronics Circuits", Fifth edition, Oxford University Press, 2009.

Web Links:	
1.	http://nptel.ac.in

Sub Title: Operating System		
Sub Code:18EC742	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understand the history and types of operating systems.
2. Understand the design issues associated with operating systems development.
3. Understand the process management and scheduling.
4. Understand the concepts of memory management.
5. Understand the file and I/O operation

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**INTRODUCTION :** Goals of an O.S, Operation of an O.S **OVERVIEW OF OPERATING SYSTEMS:**, OS and computer system, Efficiency, system performance and user convenience, Classes of operating systems, O.S and the computer system, Batch processing system, Multi programming systems, Time sharing systems, Real time operating systems. TEXT 1 .	10	L1,L2
2	**STRUCTURE OF THE OPERATING SYSTEMS:** Operation of an O.S, Structure of an operating system, Operating systems with monolithic structure, Layered design of an operating system, Virtual machine operating systems, Kernel based operating systems. TEXT1	10	L1,L2.L3
3	**PROCESS MANAGEMENT:** Process and programs, Programmer view of processes, OS view of processes, Threads. **SHEDULING:** Preliminaries, Non pre-emptive scheduling policies, pre-emptive scheduling policies, scheduling in practice. TEXT 1	11	L1,L2,L3.
4	**MEMORY MANAGEMENT:** Managing the memory hierarchy, static and dynamic memory allocations, memory allocation to a process, reuse of memory, contiguous and non contiguous memory allocation, paging, segmentation, segmentation with paging. **VIRTUAL MEMORY:** Virtual memory Basics, Demand paging, page replacement policies. TEXT 1	11	L1,L2
5	**FILE SYSTEMS:** File system and IOCS, Files and file	10	L1,L2

	organization, Fundamentals of file organizations, Directory structures, File protection, Interface between file system and IOCS, Allocation of disk space. implementation of file access. TEXT 1		

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

Course Outcomes:

CO1: Understand the evolution of operating systems and various types of operating systems in practice

CO2: Analyze the structure of operating system.

CO3: Analyze the concepts of process management and different scheduling management.

CO4: Understand the design issues in memory management and virtual meamory.

CO5: Understand the file and I/O management techniques

COs	Mapping with POs
CO1	PO1,PO2,PO4, PO12
CO2	PO2,PO3,PO4,PO10,PO12
CO3	PO1,PO2,PO3,PO6,PO7,PO12
CO4	PO1,PO2,PO4,PO11,PO12
CO5	PO1,PO2,PO11,PO12

Text Books.

D.M.Dhamdhare, "**Operating Systems**", Second Edition, TMH, 2008

Reference Text Books.

1. Stalling William, "Operating Systems", Sixth edition, Pearson Education,
2. Avi Silberchatz, Peter Baer Galvin, Greg Gagne, "Operating system Concepts", Ninth edition, John wiley & Sons

Web Links.

1. faculty.salina.k-state.edu/tim/ossg/Introduction/OSrole.html
2. https://users.dimi.uniud.it/~antonio.dangelo/OpSys/.../Operating_System_Concepts.pdf

Sub Title: Operating System		
Sub Code:18EC736	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Understand the history and types of operating systems.
2. Understand the design issues associated with operating systems development.
3. Understand the process management and scheduling.
4. Understand the concepts of memory management.
5. Understand the file and I/O operation

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**INTRODUCTION :** Goals of an O.S, Operation of an O.S **OVERVIEW OF OPERATING SYSTEMS:**, OS and computer system, Efficiency, system performance and user convenience, Classes of operating systems, O.S and the computer system, Batch processing system, Multi programming systems, Time sharing systems, Real time operating systems. TEXT 1 .	10	L1,L2
2	**STRUCTURE OF THE OPERATING SYSTEMS:** Operation of an O.S, Structure of an operating system, Operating systems with monolithic structure, Layered design of an operating system, Virtual machine operating systems, Kernel based operating systems. TEXT1	10	L1,L2.L3
3	**PROCESS MANAGEMENT:** Process and programs, Programmer view of processes, OS view of processes, Threads. **SHEDULING:** Preliminaries, Non pre-emptive scheduling policies, pre-emptive scheduling policies, scheduling in practice. TEXT 1	11	L1,L2,L3.
4	**MEMORY MANAGEMENT:** Managing the memory hierarchy, static and dynamic memory allocations, memory allocation to a process, reuse of memory, contiguous and non contiguous memory allocation, paging, segmentation, segmentation with paging. **VIRTUAL MEMORY:** Virtual memory Basics, Demand paging, page replacement policies. TEXT 1	11	L1,L2
5	**FILE SYSTEMS:** File system and IOCS, Files and file	10	L1,L2

	organization, Fundamentals of file organizations, Directory structures, File protection, Interface between file system and IOCS, Allocation of disk space. implementation of file access. TEXT 1		

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

Course Outcomes:

CO1: Understand the evolution of operating systems and various types of operating systems in practice

CO2: Analyze the structure of operating system.

CO3: Analyze the concepts of process management and different scheduling management.

CO4: Understand the design issues in memory management and virtual meamory.

CO5: Understand the file and I/O management techniques

COs	Mapping with POs
CO1	PO1,PO2,PO4, PO12
CO2	PO2,PO3,PO4,PO10,PO12
CO3	PO1,PO2,PO3,PO6,PO7,PO12
CO4	PO1,PO2,PO4,PO11,PO12
CO5	PO1,PO2,PO11,PO12

Text Books.

D.M.Dhamdhare, "**Operating Systems**", Second Edition, TMH, 2008

Reference Text Books.

1. Stalling William, "Operating Systems", Sixth edition, Pearson Education,
2. Avi Silberchatz, Peter Baer Galvin, Greg Gagne, "Operating system Concepts", Ninth edition, John wiley & Sons

Web Links.

1. faculty.salina.k-state.edu/tim/ossg/Introduction/OSrole.html
2. https://users.dimi.uniud.it/~antonio.dangelo/OpSys/.../Operating_System_Concepts.pdf

Sub Title: Real Time Embedded Systems		
Sub Code:18EC744	**No. of Credits:3=3: 0: 0 (L-T-P)**	**No. of lecture hours/week: 3**
Exam Duration: 3 hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. Introduce the fundamental concepts of the Real time Embedded systems.
2. Study concepts relating to Real time Embedded systems such as Scheduling techniques, Dynamic priority policies.
3. Describe concepts related to Multi resource services like blocking, Deadlock, live lock & soft real time services.
4. Understand the basic hardware and software components of Real time embedded systems.
5. Expose to Real time embedded system applications through different case studies.

UNIT No	Syllabus Content	No. of Hours	Bloom's Taxonomy
1	**Real-Time Embedded Systems:** Introduction, Brief history of Real Time Systems, A brief history of Embedded Systems. **System Resources:** Introduction, Resource analysis, Real-Time Service Utility, scheduling classes, Scheduler concepts, Real-Time OS. (Text 1)	07	L1,L2, L3,
2	**Processing with Real Time Scheduling:** Introduction, Pre-emptive Fixed Priority Scheduling Policies with timing diagrams, Problems and issues, Feasibility, Rate Monotonic least upper bound (No derivation), Necessary and Sufficient feasibility, Dynamic priority policies. (Text 1)	08	L1,L2, L3
3	**I/O Resources**: Execution efficiency, I/O Architecture. **Memory:** Physical hierarchy, ECC Memory, **Multi-resource Services:** Blocking, Deadlock and livelock. **Soft real-time services:** Missed deadline, QoS. (Text 1)	08	L1,L2, L3
4	**Embedded System Components:** HARDWARE COMPONENTS: Sensors, Actuators, IO Interfaces, Processor Complex or SoC, Processor and IO Interconnection, Bus Interconnection, High-Speed Serial Interconnection, Low-Speed Serial Interconnection, Interconnection Systems, Memory Subsystems. FIRMWARE COMPONENTS: Boot Code, Device Drivers, Operating System Services. (Text 1)	08	L1,L2, L3, L4,L5

5	**Case Studies:** ROBOTIC APPLICATIONS: Robotic Arm, Actuation, End Effector Path, Sensing, Tasking, Automation and Autonomy. COMPUTER VISION APPLICATIONS: Object Tracking, Image Processing for Object Recognition, Characterizing Cameras, Pixel and Servo Coordinates, Stereo-Vision. (Text 1)	08	L1,L2, L3,L6

Note:

1. Unit 1,2,3,4, and Unit 5 will have the internal choice
2. Two assignments are evaluated for 5 marks: Assignment1 – From Unit 1 and 2, Assignment2 from units 3,4 and 5

Course Outcomes:

CO1: Discuss the fundamentals of various real time services, real time service utilities, and Real time embedded system.

CO2: Apply priority based static and dynamic Real time scheduling techniques for the given real time embedded system specifications.

CO3: Analyze deadlock conditions, shared memory problem, priority inversion, missed deadlines and QoS of Real time embedded systems.

CO4: Choose the appropriate real time embedded system components to improve the performance.

CO5: Develop the simple real time embedded systems.

COs	**Mapping with POs**
CO1	PO1, PO2, PO6, PO12
CO2	PO1, PO2, PO4, PO5, PO12
CO3	PO1, PO2, PO6, PO12
CO4	PO1, PO2, PO5, PO6, PO12
CO5	PO1, PO2, PO6, PO12

Text Books.

"**Real-Time Embedded Components and Systems",** Sam Siewert, John Pratt, Mercury Learning and Information, 2016.

REFERENCE BOOKS/WEBLINKS

1. James W S Liu, "**Real Time System**", Pearson education, 2008.
2. nptel.ac.in/courses

Sub Title : OPERATIONS RESEARCH		
Sub Code: 18EC745	**No. of Credits: 3 = 3 : 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration: 3 Hours	**CIE +Assignment + SEE = 45 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course Learning Objectives: This course will enable students to:

1. To be able to understand Scope of Operations Research and TP Formulation
2. To be able to understand the Assignment Problem.
3. To be able to understand the Network Construction
4. To be able to classify the type Game Theory
5. To be able to understand the Queuing system and their characteristics

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**Introduction to Operations Research:** Basics definition, scope, objectives, phases, models and limitations of Operations Research. Transportation Problem: Formulation, solution, unbalanced Transportation problem. Finding basic feasible solutions – Northwest corner rule, least cost method and Vogel's approximation method. Optimality test.**Text1**	8	L1, L2, L3.L4
2	**Assignment model:** Formulation. Hungarian method for optimal solution. Solving unbalanced problem. Traveling salesman problem and assignment problem. **Text1**	8	L1, L2, L3.L4
3	**PERT-CPM Techniques:** Network construction, determining critical path, floats, scheduling by network, project duration, variance under probabilistic models, prediction of date of completion, crashing of simple networks. **Text1**	8	L1, L2, L3.L4
4	**Game Theory:** Formulation of games, Two person-Zero sum game, games with and without saddle point, Graphical solution (2x n, m x 2 game). **Text1**	8	L1, L2, L3.L4
5	**Queuing Theory:** Queuing system and their characteristics. The M/M/1 Queuing system, Steady state performance analyzing of M/M/ 1 and M/M/C queuing model. **Text1**	7	L1,L2,L3

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

***Course Outcomes**: The student shall be able to*

CO1: Identify the OR Definitions and Able to apply TP.

CO2. Ability to interpret and explain the Assignment Problem.

CO3. Creation of Network construction, determining critical path, floats and scheduling by network

CO4. Ability to Compare the type of 2x n, m x 2 game.

CO5. Design the Queuing system, Game Theory and their characteristics.

CO's	**Mapping with POs**	**Mapping with PSOs**
CO1	PO1,PO2,PO3,PO8,PO9,PO10	PSO1,PSO2,PS03
CO2	PO1,PO2,PO3,PO8,PO9,PO10	PSO1,PSO2,PS03
CO3	PO1,PO2,PO3,PO8,PO9,PO10	PSO1,PSO2, PS03
CO4	PO1,PO2,PO3,PO8,PO9,PO10	PSO1,PSO2, PS03
CO5	PO1,PO2,PO3,PO8,PO9,PO10	PSO1,PSO2,PS03

Text Book:	
1.	P. Sankara Iyer, "**Operations Research**", First Edition, Tata McGraw-Hill, ***2008***
2.	A.M. Natarajan, P. Balasubramani, A. Tamilarasi, "**Operations Research**", First Edition, Pearson Education, ***2005***

Reference Books:	
1.	P. K. Gupta and D. S. Hira, "**Operations Research**", Second Edition, S. Chand & co, ***2007***
2.	S D Sharma, "**Operations Research, Problems and Solutions**", Paperback 1, kedar Nath Publisher, India Ltd, ***2012***

Sub Title : **Adaptive Signal Processing**		
Sub Code: 18EC746	**No. of Credits:3=3: 0 : 0 (L-T-P)**	**No. of lecture hours/week : 03**
Exam Duration : 3 Hours	**CIE +Group Activity+Assignment + SEE = 40 + 5 + 5 + 50 =100**	**Total No. of Contact Hours :39**

Course objectives:

1. understand the basic concept of adaptive filter and adaptive system
2. identify the geometrical significance of Eigenvectors and values
3. analyse the Simple, Newton's and Steepest Descent Gradient search method to search performance surface
4. study estimation of LMS algorithm
5. familiar with design of adaptive communication system, adaptive noise canceller and adaptive modeling in FIR digital filter synthesis

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	**ADAPTIVE SYSTEMS:** Definition and characteristics, Areas of application, General properties, Open-and closed loop adaptation, Applications of closed-loop adaptation, Example of an adaptive system. (Text1)	6	L1,L2
2	**THE ADAPTIVE LINEAR COMBINER:** General description, Input signal and weight vectors, Desired response and error, the performance function, gradient and minimum mean-square error, Example of a performance surface **PROPERTIES OF THE QUADRATIC PERFORMANCE SURFACE**: Normal of the input correlation matrix, Eigen values and Eigen vectors of the input correlation matrix, an example with two weights, geometrical significance of eigenvectors and Eigen values.(Text1)	10	L1,L2,L3
3	**SEARCHING THE PERFORMANCE SURFACE:** Methods of searching the performance surface, Basic ideal of gradient search methods, a simple gradient search algorithm and its solution, Stability and rate of convergence, The learning curve, and Gradient search by Newton's method in multidimensional space, Gradient search by the method of steepest descent, Comparison of learning curves. (Text1)	10	L1,L2,L3
4	**THE LMS ALGORITHM**: Derivation of the LMS algorithm, convergence of the weight vector, an example of convergence, learning curve, noise in the weight-vector solution(Text1)	7	L1,L2,L3
5	**ADAPTIVE MODELING AND SYSTEM IDENTIFICATION:** Multipath communication channel, geophysical exploration, FIR digital filter synthesis. (Text1)	6	L1,L2

Note 1. Unit 1, 2, 3, 4 and Unit 5 will have internal choice.

Note 2.Two assignments are evaluated for 5 marks: Assignment – 1 from units 1 and 2
Assignment - 2 from units 3, 4 and 5.

Note 3.Unit 4---digital teaching and learning.

Course Outcomes:

CO1: Understand the basic concept of adaptive filter and adaptive system

CO2: Understand the design of adaptive linear combiner and Identify the geometrical significance of Eigenvectors and values

CO3: Analyse the Simple, Newton's and Steepest descent Gradient search method to search performance surface.

CO4: Estimate the gradient component using Newton's, Steepest-descent methods and LMS algorithm

CO5: Design of adaptive communication system, adaptive noise canceller and adaptive modelling in FIR digital filter synthesis.

Cos	Mapping with POs
CO1	PO1, PO2, PO3, PO4
CO2	PO1, PO2, PO3, PO4
CO3	PO2, PO3, PO4
CO4	PO2, PO3, PO4
CO5	PO5,PO6

Text Book:

1. **Bernard Widrow and Samuel D. Stearns, "Adaptive Signal Processing", Edition, Pearson Education, Asia, 2009**
2. **Simon Haykin, "Adaptive filter Theory", 4th edition, Pearson Education Asia, 2008**

Reference Books:

1. **Alexander, Thomas S, "Adaptive Signal Processing: Theory and Applications", edition, Springer-Verlag New York, Inc. New York, NY, USA, 1986**
2. **T. Adali and Simon Haykin, "Adaptive Signal Processing: Next Generation Solutions", edition, Wiley India, 2012**
3. **Jophn R. Treichler C. Richard Johnson, Jr. and Michael G. Larimore, "Theory and Design of Adaptive Filters", edition, PHI, 2002**

Web Links.

http://www.nptelvideos.in/2012/12/adaptive-signal-processing.html
http://www.cs.tut.fi/~tabus/course/ASP/Lectures_ASP.html
http://www.signal.uu.se/Courses/CourseDirs/AdaptSignTF/Adapt04. html

Active learning Assignments (AL) : Preparation of power-point slides, which include videos, animations, pictures, graphics for better understanding theory and practical work – The faculty will allocate chapters/ parts of chapters to groups of students so that the entire syllabus to be covered. The power-point slides should be put up on the web-site of the College/ Institute, along with the names of the students of the group, the name of the faculty, Department and College on the first slide. The best three works should submit to ECE Department, Dr. AIT.

Sub Title : Advanced Communication Lab		
Sub Code: 18ECL76	**No. of Credits: 01=0 : 0 : 1 (L-T-P)**	**No. of lecture hours/week: 02**
Exam Duration : 3 Hours	**CIE + SEE = 50 + 50 =100**	**Total No. of Contact Hours :30**

Course objectives:

1. Understand the circuit schematic and its working of ASK, FSK, PSK, DPSK and QPSK circuits.
2. Design and test of ASK, FSK, PSK, DPSK and QPSK circuits.
3. Analyzing various losses using OFC kit
4. Measurement of parameters like frequency, guide wavelength, power, VSWR and Attenuation.
5. Learn to measure directivity and gain of different antennas.
6. Demonstrate sampling theorem under different sampling conditions.

Experiment No	Laboratory Experiments	No of Hours	Blooms Taxonomy level.
	Part A: Hardware Experiments		
1	ASK generation and detection using discrete components.	2	L1, L2, L3. L4
2	FSK generation and detection using discrete components.	2	L1, L2, L3. L4
3	PSK generation and detection using discrete components.	2	L1, L2, L3. L4
4	To prove sampling theorem, to study the effects of under sampling and oversampling.	2	L1, L2, L3. L4
5	DPSK generation and detection using kit.	2	L1, L2, L3. L4
6	QPSK generation and detection using kit	2	L1, L2, L3. L4
7	Establish Analog and Digital communication link using optical fiber and Measure the losses (coupling loss, bending loss, attenuation loss numerical aperture.)	2	L1, L2, L3. L4
8	Measurement of frequency, guide wavelength, power, VSWR and Attenuation in a microwave test bench.	2	L1, L2, L3. L4
9	Measurement of directivity and gain of micro strip patch antenna using printed dipole.	2	L1, L2, L3. L4
10	Measurement of directivity and gain of Yagi antenna (printed) using printed dipole.	3	L1, L2, L3. L4

Course Outcomes: After the completion of the Course the student are able to:

CO1. Understand the working of ASK, FSK, PSK, DPSK and QPSK circuits.
CO2. Design ASK, FSK, PSK, DPSK and QPSK circuits.
CO3. Analyse various losses using OFC kit and parameters like frequency, guide wavelength, power, VSWR and Attenuation.
CO4. Demonstrate the sampling theorem and measurement of antenna parameters.

Cos	Mapping with POs	Mapping with PSOs
CO1	PO1, Po4,PO8,Po12	PSO1,PSO2
CO2	PO1,PO2,PO3,PO4,PO8,PO12	PSO1,PSO2
CO3	PO1,PO2,PO3,PO4,PO5,Po5,PO12	PSO1,PSO2

Reference Books:	
1.	Digital Communication: Sam Shanmugam, WILEY INDIA,2008
2.	ANTENNA THEORY: ANALYSIS AND DESIGN, 3RD ED (With CD), John Wiley & Sons, 2009

Web Links:	
1.	www.nptel.in

Sub Title : COMPUTER COMMUNICATION NETWORK LAB		
Sub.Code: 18ECL77	**No. of Credits:01=0:0:1(L - T –P)**	**No. of Lecture Hours/Week : 03**
ExamDuration: 03Hrs	**CIE + SEE = 50 + 50 =100**	**Total No.of Contact Hours:13**

Course objectives:

1. students should be able to demonstrate the simulation of few protocols of data link layer and network layer.
2. students should be able to demonstrate the network communication between source and destination.
3. students should be able to demonstrate the detection and correction of error in data communication.
4. students should be able to demonstrate the data communication between the systems using different media.

UNIT No	Syllabus Contents	No of Hours	Blooms Taxonomy level.
1	Write a C program to implement Bit Stuffing and deStuffing	03	L1,L6
2	Write a C program to simulate a character stuffing and destuffing for a given message.	03	L1,L6
3	Write a C program to compute a polynomial checksum for a given binary data frame	03	L1,L6
4	Write a C program to simulate a shortest path Algorithm.	03	L1,L6
5	Using TCP/IP Sockets, write a client-server program to make client to communicate with Server using socket programming techniques in python.	03	L1,L6
	PART-B		
6	**SERIAL COMMUNICATION USING** (i) RS232 (ii) MODEM COMMUNICATION (iii) FIBER OPTIC COMMUNICATION	03	L4,L5
7	**Configuring and Verifying LAYER 2 Switches:** Establish a communication between the HOSTS by connecting the Network Devices as given below, configure them and verify the same. Configuration includes HOSTNAME, BANNER, PASSWORD (CONSOLE, TELNET and ENABLE),MANAGEMENT IPand DEFAULT GATEWAY.	03	L3,L4,L5
8	**Configuring and Verifying VLAN:**Establish a communication between the hosts by connecting the network Devices as given below, configure them and verify the same. Configuration includes Switch port configuration and encapsulation methods.	03	L3,L4,L5
9	**Configuring and Verifying IP Routing:**Establish a communication between the hosts by connecting the network Devices as given below,	03	L3,L4,L5

	configure them and verify the same. Configuration includes: 1. Static Routing 2. Dynamic Routing (RIP/OSPF/EIGRP)		
10	**Configuring DHCP Server on a Router:** Configure DHCP server on a router to assign IP address dynamically to the hosts and verify the same **a. For One Broadcast Domain** **b. For Many Broadcast Domain**	03	L3,L4,L5
11	**PART-C [Simulation Case-Study]** Dr. AIT is granted a block of addresses starting from **192.168.100.0/24**. The Dr. AIT College committee decided to distribute these blocks of addresses to **THREE** Departments with each department receiving just **FOUR** Addresses. **1. Design the sub blocks and give the slash notation to each sub block.**	03	L3,L4,L5
12	**2. Simulate the above case using Cisco-packet Tracer.** Note: while simulating Consider the following Constraints: a. Establish a communication within the Departments. b. Only HOD's of each Department can communicate (Single user from each Department) with each other.	03	L3,L4,L5
13	Create topology to demonstrate port security using any application layer protocol.	03	L3,L4,L5

	Programme Outcomes (POs)
1	After the successful completion of this course the student should be able to conduct an experiment to simulate various protocols of data link and network layer.
2	After the successful completion of this course the student should be able to demonstrate the data communication between two systems using the communication kit.
3	After the successful completion of this course the student should be able to write the programs to verify the detection and correction of error.
4	After the successful completion of this course the student should be able to verify the algorithm to find shortest path.

	Relationship to the Program Outcomes(POs)	
	Course Outcomes (COs)	**Program Outcomes (POs)**
	CO1	PO4,PO5,PO9
	CO2	PO4,PO5,PO9
	CO3	PO4,PO5,PO9
	CO4	PO4,PO5,PO9
	CO5	PO4,PO5,PO9

Dr. Ambedkar Institute of Technology, Bengaluru-560 056

SCHEME OF TEACHING AND EXAMINATION from Academic Year 2020-21

B.E in Electronics and Communication Engineering

Outcome Based Education (OBE) and Choice Based Credit System (CBCS) (Applicable to 2018 Batch)

VIII Semester

Sl. No	Course and Course Code		Course Title	Teaching Dept.	Teaching Hours / Week			Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Drawing / Practical (P)	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	MC	18CV81	Occupational and Safety and Health administration	CV	02	--	--	03	050	050	100	02
2	PRJ	18ECP83	Project Work Phase-2	EC	--	--	02	03	050	050	100	10
3	Seminar	18ECS84	Technical Seminar	EC	--	--	02	03	050	050	100	01
4	INT	18ECI85	Industry Internship	EC	--	--	--	03	050	050	100	02
				Total	**05**	**--**	**04**	**15**	**250**	**250**	**500**	**15**

Internship: Those, who have not pursued /completed the internship will be declared as failed and have to complete during subsequent SEE examination after they satisfy the internship requirements.

Note: : PC: Professional Core. PE: Professional Elective, OE: Open Elective. MC: Mandatory Course, PRJ: Project work, INT: Internship

Select **ANY ONE** of the Professional Elective and Open Elective subject

Students can select any one of the open electives (Please refer to consolidated list of Dr. AIT open electives) offered by any Department.
Selection of an open elective is not allowed provided,

- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of Departmental core courses or professional electives. Registration to electives shall be documented under the guidance of Programme Coordinator/ Mentor.

Syllabus for 2018-19 Batch UG (CV)

Semester: VII / VIII	
Course Title: OCCUPATIONAL SAFETY AND HEALTH ADMINISTRATION (OSHA)	
Course Code: **18HS72 / 82**	Evaluation Procedure:
Credits: **02**	CIE + Assignment + Group Activity + SEE Marks = 40 + 5 + 5 + 50 = 100
Teaching Hours: 26 Hrs. (L:T:P:S) - 2:0:0:0	SEE Duration: 2 Hrs

Course Learning Objectives:	
1	To gain an historical, economic, and organizational perspective of occupational safety and health.
2	To investigate current occupational safety and health problems and solutions.
3	To identify the forces that influence occupational safety and health.
4	To demonstrate the knowledge and skills needed to identify work place problems and safe work practice.

UNIT - I	
OCCUPATIONAL HAZARD AND CONTROL PRINCIPLES: Safety, History and development, National Safety Policy. Occupational safety and Health Act (OSHA), Occupational Health and Safety administration - Laws governing OSHA and right to know. Accident – causation, investigation, investigation plan, Methods of acquiring accident facts, Supervisory role in accident investigation.	**6 Hrs**
UNIT - II	
ERGONOMICS AT WORK PLACE: Ergonomics Task analysis, Preventing Ergonomic Hazards, Work space Envelops, Visual Ergonomics, Ergonomic Standards, Ergonomic Programs. Emergency Response - Decision for action – purpose and considerations.	**5 Hrs**
UNIT - III	
FIRE PREVENTION AND PROTECTION: Fire Triangle, Fire Development and its severity, Effect of Enclosures, early detection of Fire, Classification of fire and Fire Extinguishers. Electrical Safety.	**5 Hrs**
UNIT – IV (Blended Learning)	
HEALTH CONSIDERATIONS AT WORK PLACE: Types of diseases and their spread, Health Emergency. Personal Protective Equipment (PPE) – types and advantages, effects of exposure and treatment for engineering industries, municipal solid waste. Environment management plans (EMP) for safety and sustainability.	**5 Hrs**
UNIT - V	
OCCUPATIONAL HEALTH AND SAFETY CONSIDERATIONS: Handling of chemicals and safety measures in water and wastewater treatment plants and labs, Construction material manufacturing industries like cement plants, RMC Plants, precast plants and construction sites. Policies, roles and responsibilities of workers, supervisors and managers.	**5 Hrs**

Course Outcomes: The students will be able to	
1	Acquire knowledge on OSHA policies, Laws and regulations.
2	Identify hazards in the workplace that pose a danger or threat to the safety or health, or that of others.
3	Control unsafe or unhealthy hazards and propose methods to eliminate the hazards.
4	Discuss the role of health and safety in the workplace and effects of industries on environment.
5	Identify workplace hazards, safety considerations and roles and responsibilities of workers, supervisors and managers.

Question paper pattern:
• Each unit has two full questions with internal choice. • Each full question will have a maximum of two sub question. • Each full question will be for 10 Marks. • Students will have to answer five full questions, selecting one full question from each unit.

Text Books:	
1	S Sharma, Vineet Kumar, "Safety, Occupational Health and Environmental Management in Construction". Khanna Publisher, 2013.
2	R K Jain, Sunil S Rao, "Industrial Safety, Health and Environment Management Systems". Createspace Independent Publishing Flat form, 2000.
3	Charles D Reese, "Occupational Safety and Health Fundamental principles and Philosophies", Tailor and Francis Ltd, 2017.
4	Sudhakar Paul T Rani, "Occupational Safety and Health", Createspace Independent Publishing Platform, 2018.
5	Akhil Kumar Das, "Principles of Fire Safety Engineering-Understanding Fire and Fire Protection-", PHI Learning Pvt. Ltd, 2019.
6	Lakhwinder Pal Singh, "Work study and Ergonomics", Cambridge University Press, 2018.
7	Industrial safety Sectional Committee CHD8, IS-14489:2018; Occupational Health and Safety Audit- Code' of Practice (First Revision) Bureau of Indian Standards.

Reference Books:	
1	Mishra R K, "Safety Management", AITBS Publisher.
2	Rana S P, Goswami P K, and Indu Rathee, "Handbook of Occupational Safety and Industrial Psychology". S. Chand and Company Ltd, 2014.
3	Narayanaraju G (Secretary to GOI), "The Occupational Safety, Health and Working Conditions Code, 2020", NO. 37 OF 2020, Govt. of India, Ministry of Law and Justice.
4	Goetsch D. L., "Occupational Safety and Health for Technologists, Engineers and Managers", Prentice Hall Publishers, 2010.

CO-PO Mapping

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓											
CO2					✓							
CO3					✓							
CO4							✓					
CO5									✓			✓